Getting Started With Circuit Envelope

Introduction

This page helps to take a DUT that is working in Harmonic Balance and verify that it gives the same results with a CW signal in the Circuit Envelope simulator. If assistance is needed with modulated signal analysis contact your local Application Engineer our the AWR support team.

Requirement

- **AWR Design Environment V14 (or greater)**
- You will typically run circuit envelope on an amplifier, mixer or modulator circuit
- The circuit must be a fully functional non-linear Microwave Office circuit that runs in APLAC

Think Time Domain

It is important to remember that Circuit Envelope is a time domain technique. Often the circuits that people generally want to use in Circuit Envelope are not well suited for the time domain. PAs, in particular, are a likely candidate for Circuit Envelope because there are all kinds of exotic linearization schemes in use that can only be simulated in a time domain engine; unfortunately, they are often constructed with models that don't map well (or cleanly) into the time domain. These include chip cap models, undersampled or low-frequency s-parameters, and microstrip lines with extreme (> 30) width to height ratios.

Element Limitations

The Circuit Envelope development cycle resulted in many time domain model mapping improvements, but not all elements can be supported in the time domain. If the design contains a model that does not work in the time domain the simulation will generate an error. Please contact AWR technical support is this happens. And, of course, since we're talking about APLAC simulators, **all the models must work in APLAC.** Contact AWR technical support to resolve model issues.

Initial Setup

Start this procedure from your currently working amplifier project.

Running Your Circuit With Time Domain Models

There's a very simple test to see if the circuit in question can be correctly converted to the time domain. When AWRDE netlists to APLAC Harmonic Balance it sends a frequency domain netlist (MLINs, s-parameters, etc.) and when it netlists to APLAC Transient it uses a time domain netlist (rational approximations, w-elements, etc.). The first test is to send a time domain netlist to a frequency domain simulation engine (i.e. send a Transient netlist to Harmonic Balance). Why? Because HB runs quickly and shows if there are any time domain model mapping issues.

To start, open the project that contains circuit you want to run in Circuit Envelope

Push the button below to import an AM to AM test bench.

Import AM

In the "CE Cookbook" Global Definitions Document you need to:

1. Set the simulation frequency
2. Set the power sweep

In the "CE Cookbook AM to AM" Circuit Schematic you need to

1. Place a subcircuit of your DUT and wire it up (including bias)

Push the button below to duplicate the Circuit Envelope Cookbook AM to AM Circuit Schematic, configure the copy to generate a transient netlist, add a Graphs and Measurements for AM to AM and AM to PM, and run the simulation.

Run HB A

Did you get any simulation errors? Were there model mapping errors? If it does simulate how does it compare to the original Harmonic Balance simulation?

The steady-state waveforms or AM to AM and AM to PM measurements should be nearly identical and, of course, reflect the expected device behavior. If the results are not good please contact AWR Technical Support.

Running Your Circuit With Circuit Envelope

Now that the simple time-domain test is done it's time to a simple test your circuit using the Circuit Envelope Simulation engine. This step compares the Circuit Envelope AM to AM and AM to PM response with the results from the test benches in the steps above. Push the button below to add a new Circuit Envelope AM to AM and AM to PM measurement to the Graphs and simulate your design using the Circuit Envelope engine.

Run CE A

Similar to the step above, did you get any simulation errors? Were there model mapping errors? If it does simulate how does it compare to the original and time domain model Harmonic Balance simulation?

As before, the steady-state waveforms or AM to AM and AM to PM measurements should be nearly identical and, of course, reflect the expected device behavior. If the results are not good please contact AWR Technical Support.

If you plan to use Circuit Envelope directly on Circuit Schematics then there's no need to continue the next step. If desired, you can remove all of the Circuit Envelope Cookbook created content in the Clean Up section. However, if you need to co-simulate with VSS and Circuit Envelope then please continue to the "Setting Up the Circuit Test Bench for VSS And Circuit Envelope Co-Simulation" section below.

Setting Up the Circuit Test Bench For VSS and Circuit Envelope Co-Simulation

Setting up VSS and Circuit Envelope co-simulation requires the VSS NL_S_ENV. The big question is "what do you want to do in VSS?" Just drive it with a modulated signal and look at the resulting waveform? Monitor or control DC and/or RF voltages and currents from VSS. Once you know the connections you want you just need to get ports attached appropriately.

- RF Inputs and outputs are defined with a PORT element connected to the input and output nodes
- DC voltages (either in probe or source configuration) are defined with a PORT element connected at the desired probe/source location
    - For DC voltage probes the V_METER2 element makes probing the circuit easy and PORT element attaches to pin 3 to pass the voltage to VSS
- DC currents (either in probe or source configuration) are defined with a PORT element connected at the desired probe/source location
    - For DC current probes the I_METER2 element is required and a PORT element attaches to pin 3 to pass the current to VSS

Final Sanity Check

There is one final step before using the NL_S_ENV signal with a modulated signal and that's to compare VSS AM to AM and AM to PM with the results from the test benches in the steps above. Push the button below to import a System Diagram for AM to AM and AM to PM verification using Circuit Envelope, add a system AM to AM and AM to PM measurement to the Graphs, and run VSS.

Import VS

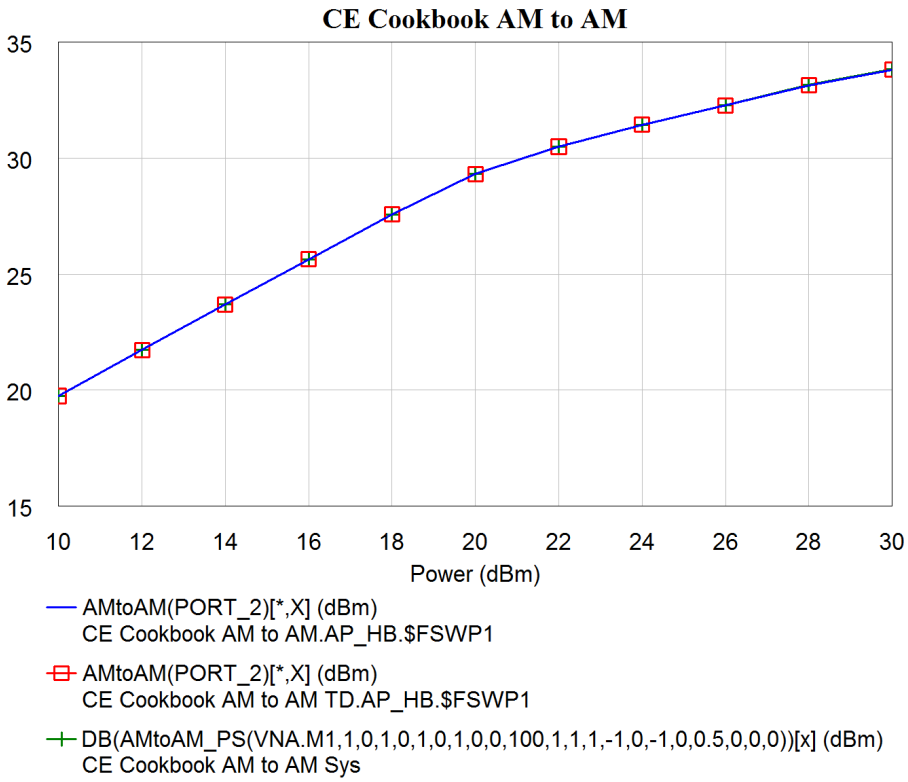
Compare Results

After the VSS simulation is complete the AM to AM and AM to PM graphs should contain curves from APLAC Harmonic Balance, APLAC Harmonic Balance using a time domain netlist, and VSS with Circuit Envelope as shown below (click to see larger image).

As before, all of the data should be a very close match. If the results are not good please contact AWR Technical Support.

If desired, you can remove all of the Circuit Envelope Cookbook created content in the Clean Up section.

Sample Results (Click to see larger image)



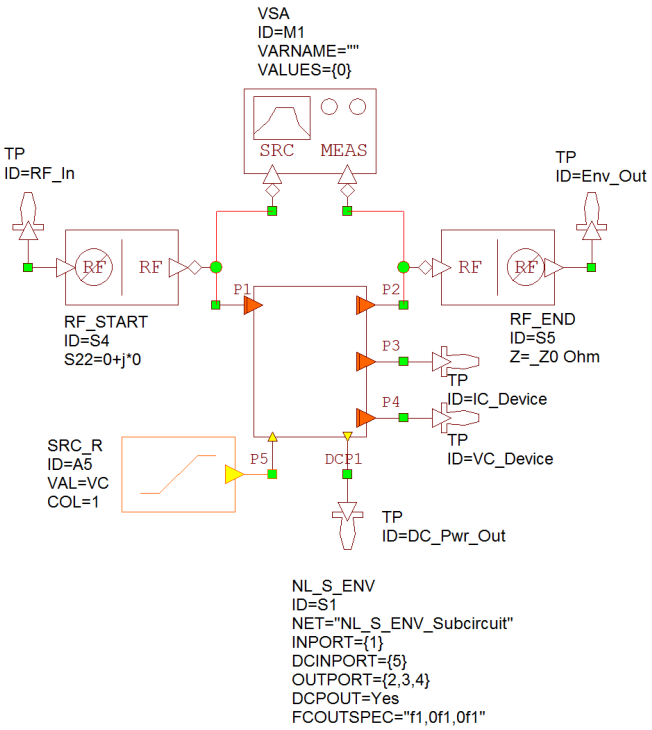
Additional Information

Configuring The NL_S_ENV Element

The NL_S_ENV element has a great help page so there's no need to duplicate that information here. However, a quick overview probably makes sense. On the NL_S_ENV there are vectors of MWO port numbers to describe RF input pins, DC input pins, and output pins. For the output pins, there's another vector which tells which harmonic should come back into VSS (0 for DC, F1 for fundamental, 3F1 for 3rd harmonic, etc.). And, lastly, there's an optional DC output power node that can be exposed to look at PAE under modulated drive. The symbol, in an attempt to be as helpful as possible, displays the corresponding MWO port numbers rather than the VSS pin numbers (it's dynamic so you can't change it) after the pin arrays are configured.

Remember that **RF blocks (the ones with the little diamond on the symbol pins) groups must be surrounded by RF_START and RF_END blocks to work properly** as shown in the picture below (click to see larger image). Also, **to properly do any measurement that could be delay sensitive (EVM, constellation, etc.) requires the ALIGN block** (VSS standard operating procedure). Lastly, I recommend the PWR_MTR measurement to always verify the input test point. If the answers look odd or unintuitive please make sure that the NL_S_ENV block is configured correctly.

NL_S_ENV Setup (Click to see larger image)



Clean Up

If desired the button below will clean up all the Circuit Schematics, System Diagrams, Global Definitions, and Graphs created by the cookbook

Remove (