Passive_FETQ_Mixer

Where To Find This Example

Select **Help > Open Examples...** from the menus and type either the example name listed above or one of the keywords below.

Or in Version 13 or higher you can open the project directly from this page using this button. Make sure to select the **Enable Guided Help** before clicking this button.

Open Install Example

Design Notes

Passive FETQ (FET Quad) Mixer

The Passive FETQ (FET Quad) Mixer is a classical mixer constructed from 4 FETs connected in a ring. It is identical to the upper 4 transistors in the classical Gilbert mixer. The fundamental difference is obviously we do not use the 2 lower RF input devices biased actively for gain. We are simply using the 4 LO switching transistors and biasing them in the off state, therefore using the term “passive” to describe the bias condition. In using the passive bias condition, the LO waveform is periodically turning on the FET to modulate the gate channel conductance. In other words, the channel conductance is switching on and off at the rate of the LO signal. This gives the mixing operation since the IF current is proportional to the multiplication of the RF signal injected at the source and the conductance of the channel (now a waveform modulated at the LO frequency). One final note, we have installed a bias on the gate of VG = 1 V (defined in Global Definitions with a variable VG). Other bias conditions can be explored and the circuit re-optimized to give possibly better results. This was not exhaustively researched in this example.

Overview

This project consists of 5 separate schematics:

1. CL_and_IRL

This is the primary schematic used to measure the Conversion Loss and Input Return Loss.

2. ORL

This is a separate schematic used to measure Output Return Loss. It is

necessary because we must inject a signal into the output under LO excitation in order to measure the large signal return loss.

3. LO_Pwr_Swp

LO_Pwr_Swp is used to sweep LO power while measuring conversion loss and input return loss.

4. RF_Pwr_Swp

RF_Pwr_Swp is used to sweep the input power to obtain the compression point of the mixer.

5. transformer

This schematic was used to verify the correct operation of the transformers.

Optimization

Optimization was used to obtain the best turns ratios of the transformers used on the ports of the mixer. Here we used 100 iterations of the Pointer-Robust method.

Measurements

There are 5 graphs used in the project:

1. Conversion Loss and Input Return Loss

Notice all the measurements used for the mixer are non-linear measurements. There are no linear measurements performed on the mixer because by definition, the physical mixing operation described previously is non-linear. Here we are using LSSnm (large signal s-parameter) measurements.

2. Output Return Loss

3. CL vs LO PWR

4. CL vs RF PWR

    Notice the Input P1dB is 14 dBm.

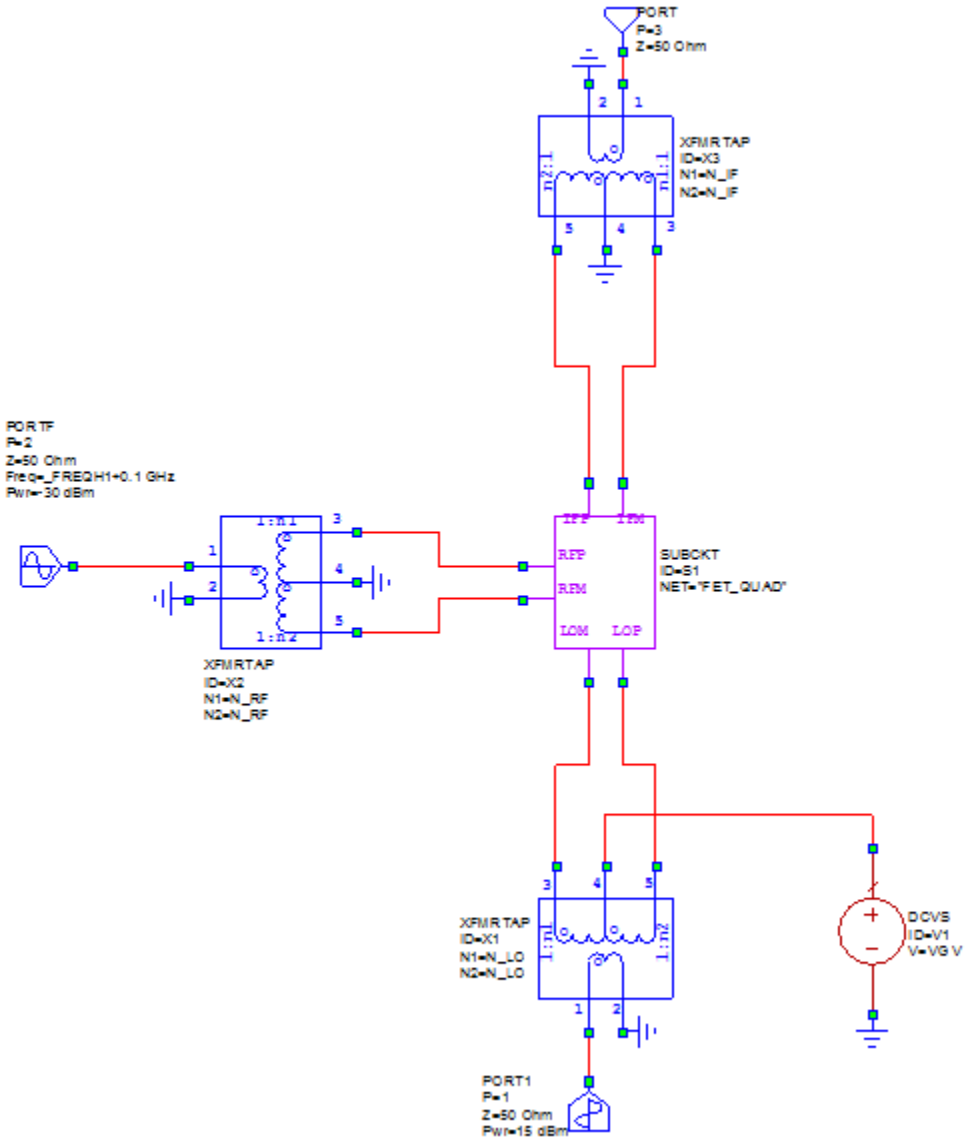
5. transformer

The transformer was characterized using linear s-parameter measurements.

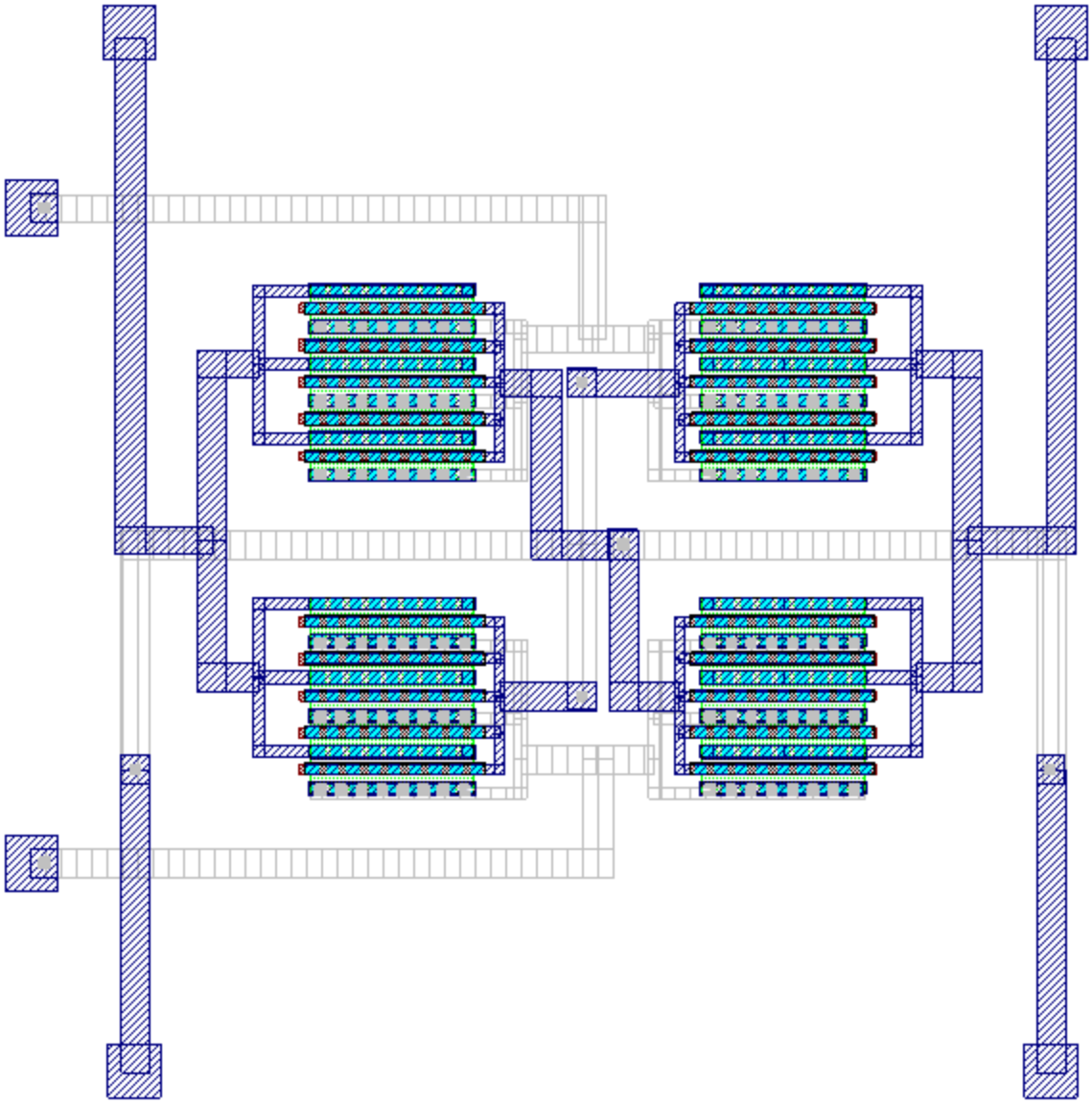
Conclusion

The passive FET mixer is a common circuit topology, but has been difficult to design due to its highly non-linear operation. With this project template, it becomes a simple exercise. The primary advantage of the passive FET mixer is the superior capability with the correct design to obtain high linearity. But, most often the designer will not be able to simulate IP3 directly due to the difficulty of obtaining non-linear device models from the foundry. The foundry will often readily supply “active” non-linear models (devices biased in the active region), but likely those same models will not model the “passive” non-linear behavior. If we attempt to simulate IP3 in this project, the results will not be consistent vs linear input power and cannot be trusted. However, we use the estimated linearity approach by measuring the 1 dB compression of the mixer (1st order effect) and apply the 10 dB rule to estimate the IP3 = P1dB +10. In this particular optimized condition, we see P1dB = 14 dBm which gives estimated IIP3 = 24 dBm.

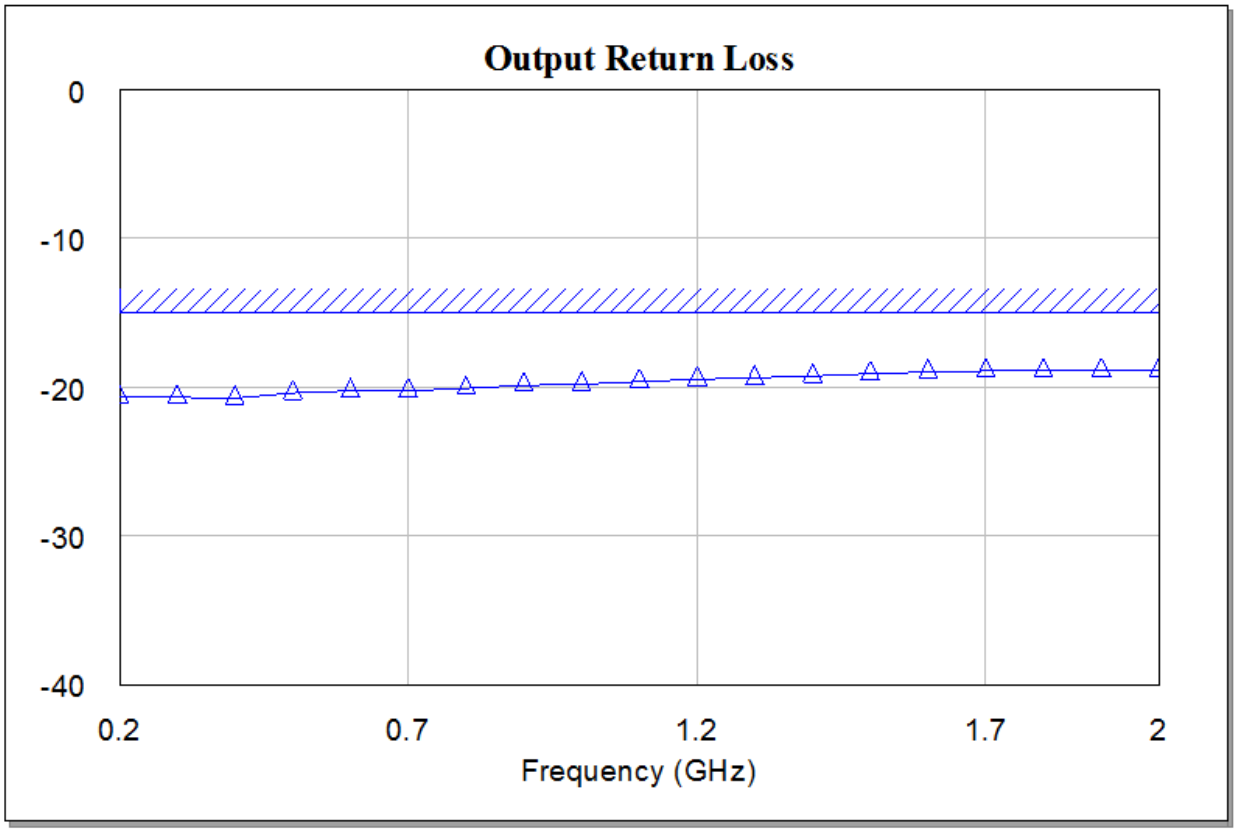
Schematic - CL_and_IRL



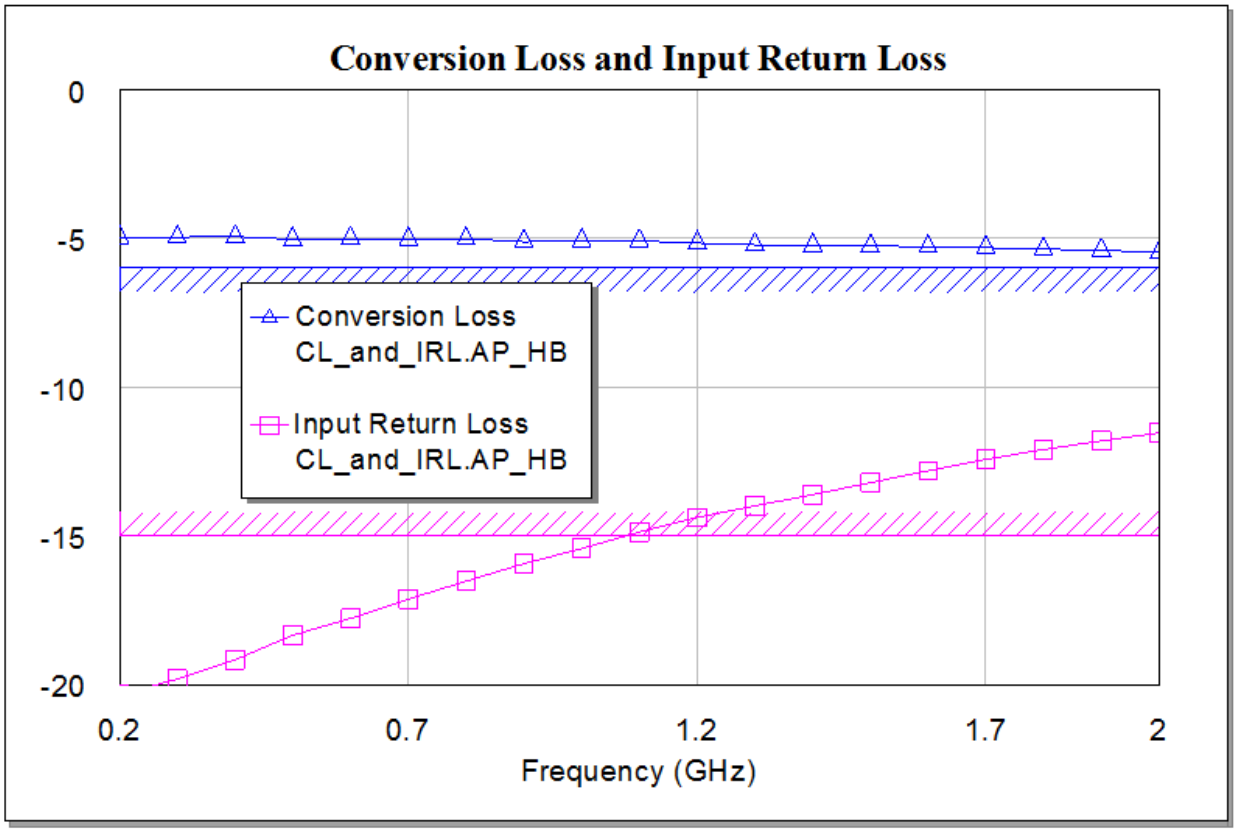
Schematic Layout - FET_QUAD



Graph - Output Return Loss



Graph - Conversion Loss and Input Return Loss



Graph - Conversion Loss vs RF PWR