**Time_Delay**

**Where To Find This Example**

**AWR Version 14**

This example was removed in V14.

**AWR Version 13**

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Understanding AWR .emz Files

**Design Notes**

**How to Measure Time Delay of a Network**

**Overview**

This simple example shows various ways to measure the time delay of a network. There are two situations, a matched network and an unmatched network. For this example, we are using an ideal transmission line where we can set the electrical length and impedance of the line. The electrical length is set to variable defined in the global definitions and setup for tuning. You can tune this electrical length and see the effects of both the matched and unmatched cases.

You can always attempt to match a network by varying the port impedance until there is minimal reflection from that network. This is a general way to find the characteristic impedance of a line.

In this example, we have set an electrical length of 36 degrees at 1 GHz. This is 10% of a wavelength and a 1 GHz sine wave has a time of 1ns. So this line should have a time delay of 0.1 ns. The schematic "Matched_Line" is perfectly matched 10 ohm line. The schematic "Unmatched_Line" is a 10 ohm line in a 50 ohm system.

**Approach 1**

The simplest approach is to just measure the group delay of the line. Please see the "Group Delay" graph for this data. The issue with this approach is that the line must be matched to get an accurate delay. Notice how the unmatched case will not give you the right answer. If you have a simple line structure that is a constant impedance along the line, you can set (you can tune or opt for minimum reflection to find this value also) the port impedances to the characteristic impedance and then measure group delay to get the time delay.

**Approach 2**

You can use Time Domain Reflectometry (TDR) to get an idea of the time delay. This only requires the linear simulator to get this information. See the "Time Domain Reflectometry" graph to see the results for both a matched and unmatched cases. In both cases, the main spike is the time delay of the network. Notice how this does not have any effect on being matched for this case. You will have to be careful setting up the frequencies of simulation for the TDR measurements to make sure you get enough time resolution. The highest frequency will set the time resolution and the frequency step will set the maximum time. Hopefully you have a basic idea of how long your line is before you start.

**Approach 3**

You can use a voltage pulse at the input and measure the voltage at the output and calculate a delay. This will require a nonlinear simulator to produce the voltage sources for this simulation. Please see the schematic "Pulse_Matched" and the graph "Pulse Matched" to see the results for the matched case. Notice the markers showing the time delay for the rising edge of the pulse, the difference in time is 0.1 ns. The schematic "Pulse_Unmatched" and graph "Pulse Unmatched" show the results for the unmatched case. Due to reflections and harmonic balance being a steady state simulator, you will have multiple pulses at the output (remember that harmonic balance always shows two period of the waveforms in the AWRDE). In this case, the largest one will be the main pulse at the output.

There are several issues to be aware of with this approach. You need to have many harmonics to get a nice clean pulse signal. We are using 1024 harmonics in this case. Since this is a linear only simulation, that many harmonics is not a problem. We have also set the pulse frequency to be 1 GHz (set as the project frequencies) and a pulse width of 0.05 ns (so it is 1/20th of the period), this make the display look nice and easier to find the edges. This works well for this electrical length at 1 GHz. You would probably want to adjust your frequency and keep your pulse width 1/20th of the frequency such that the line is no more than quarter wavelength at the frequency you have chosen. You can watch how this can get confusing if you tune the electrical length over 180 degrees and trying to find the main signal at the output.

**Conclusion**

Based on this study, TDR is the best way to find the time delay of a line matched or unmatched since it only requires linear simulation and the setup is relative easy (just need to get the frequencies right to get enough time resolution and time span.

**Schematic - Pulse_Unmatched**
PORT_PLS
P=1
Z=50 Ohm
AMP=1 V
TW=.05 ns
TR=0 ns    ISOL8R
TF=0 ns    SUBCKT
TD=0 ns    ID=U1
R=50 Ohm   ID=S1
WINDOW=BLC
OFFSET=0 dB
ISOL=30 dB
DCVal=0 V

Schematic - Pulse_Matched
PORT_PLS
P=1
Z=10 Ohm
AMP=1 V
TW=.05 ns
TR=0 ns
TF=0 ns
TD=0 ns
WINDOW=BLACK
Offset=0 V
DCVal=0 V

SUBCKT
ID=S1
NET="Matched_Line"

PORT
P=2
Z=10 Ohm

Graph - Group Delay
Graph - Pulse Unmatched