

Modelithics_Example

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AWR Version 15

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Design Notes

Modelithics Example

PDK

You must first install the Modelithics Select Library to properly simulate this example. You can obtain this library from AWR downloads page under "Vendor Libraries" tab.

Overview

This example takes advantage of the CLR library of surface mount components, an add-on library developed by AWR Alliance partner, Modelithics. This library is sensitive to PCB substrate material--especially at higher frequencies--and accurately models package resonances and the effect of SMT pad metal properties. This sample library is available in AWR's Library section, no download or install required.

In this example, a simple bias network is created and laid out with Modelithics parts. After routing, a critical net is analyzed using extraction to Axiem to get a more accurate interconnect model. The more accurate interconnect model is compared with the original circuit model based schematic and non-Modelithics based schematic.

The simulation run is from 100MHz to 10GHz to simulate the kind of broadband performance that you might expect in the signal path of a digital communications circuit.

Schematic Bias Circuit Based

This is the baseline schematic and uses 3 Modelithics parts: a Murata capacitor, a Coilcraft inductor, and an ATC capacitor. The circuit is routed by hand, using MCTRACEs, to purposefully create a structure which would be expected to have significant EM coupling not handled by the analytically MLIN and MCURVE models making up the electrical model of the MCTRACE.

Schematic Bias EM Based

This schematic was constructed by:

1. Drag-and-drop a copy of the "Bias Circuit Based" schematic onto the "Circuit Schematics" node of the MWO project palette.
2. Add **Extract Block** and **Stackup** to the new schematic, and configure them for Axiem simulation.
3. Enable desired circuit elements for Extraction. Elements enabled for extraction will highlight when clicking on the **Extract Block**.
4. Add Extraction Ports to Schematic Layout. Select Shape in Layout, from menu select **Draw > Extraction Port**, and click on shape edge to add Port. Extraction Ports allow EM Port options such as numbering and de-embedding to be set up in the schematic layout, and then are applied to the Extracted Document. In the schematic layout for "Bias_EM_Based", note that a reference plane distance has been specified for Port 3, and that Port 4 and Port 5 are using Mutual Group De-embedding. The corresponding Ports in the extracted document "EM_Extract_RF_Thru" have inherited their port properties from the Extraction Ports in the schematic layout.

Schematic Bias No Modelithics

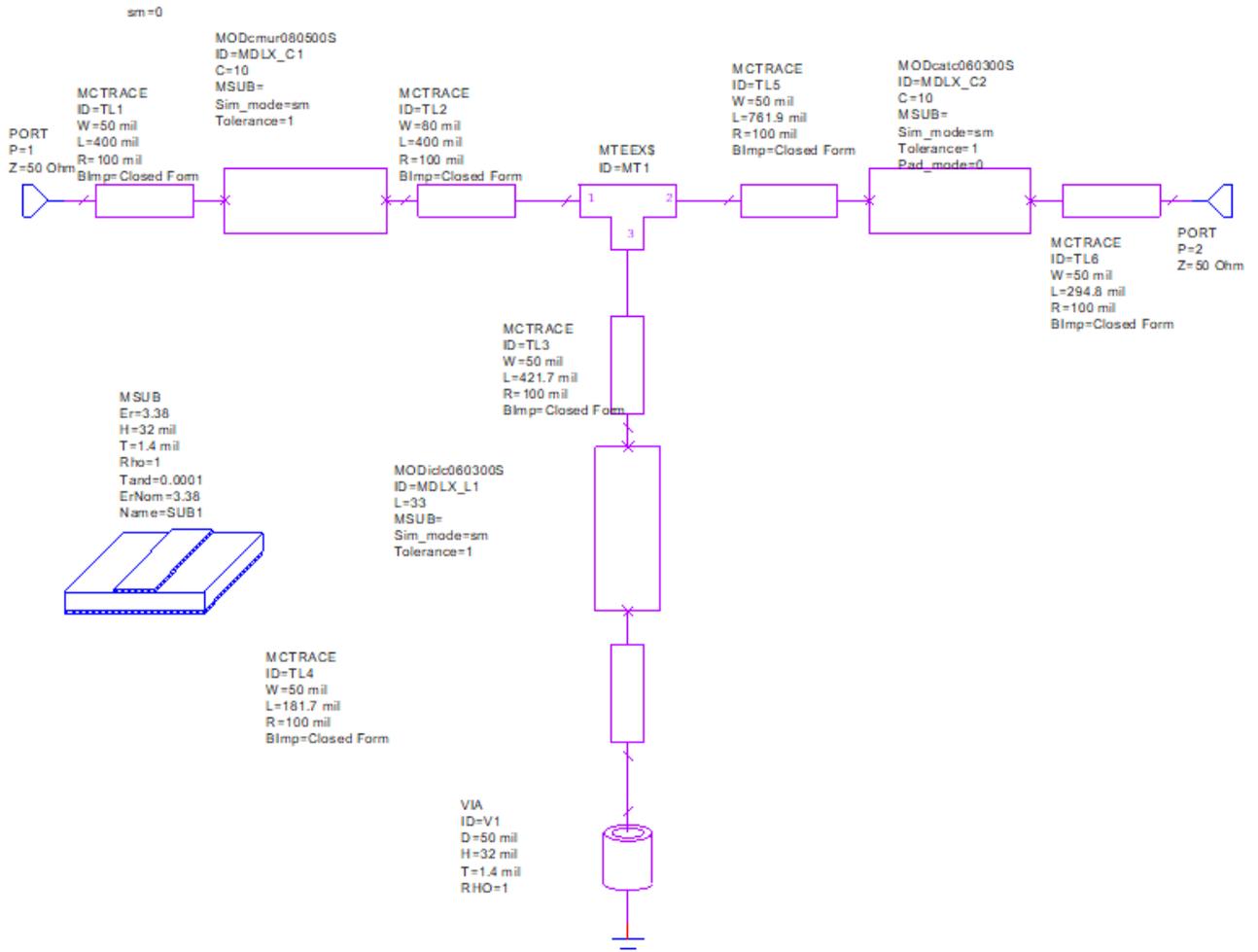
This schematic uses CAPQ and INDQ models with nominal values of Q=100 at 1GHz in place of the more accurate and precise Modelithics models. The schematic "Bias Circuit Based" has a variable named "sm" that controls how the Modelithics models simulate the PCB parasitics. With "sm=0", the PCB parasitics are simulated. Change "sm=1" to simulate without parasitics and see that these results now match the results not using Modelithics models.

Summary

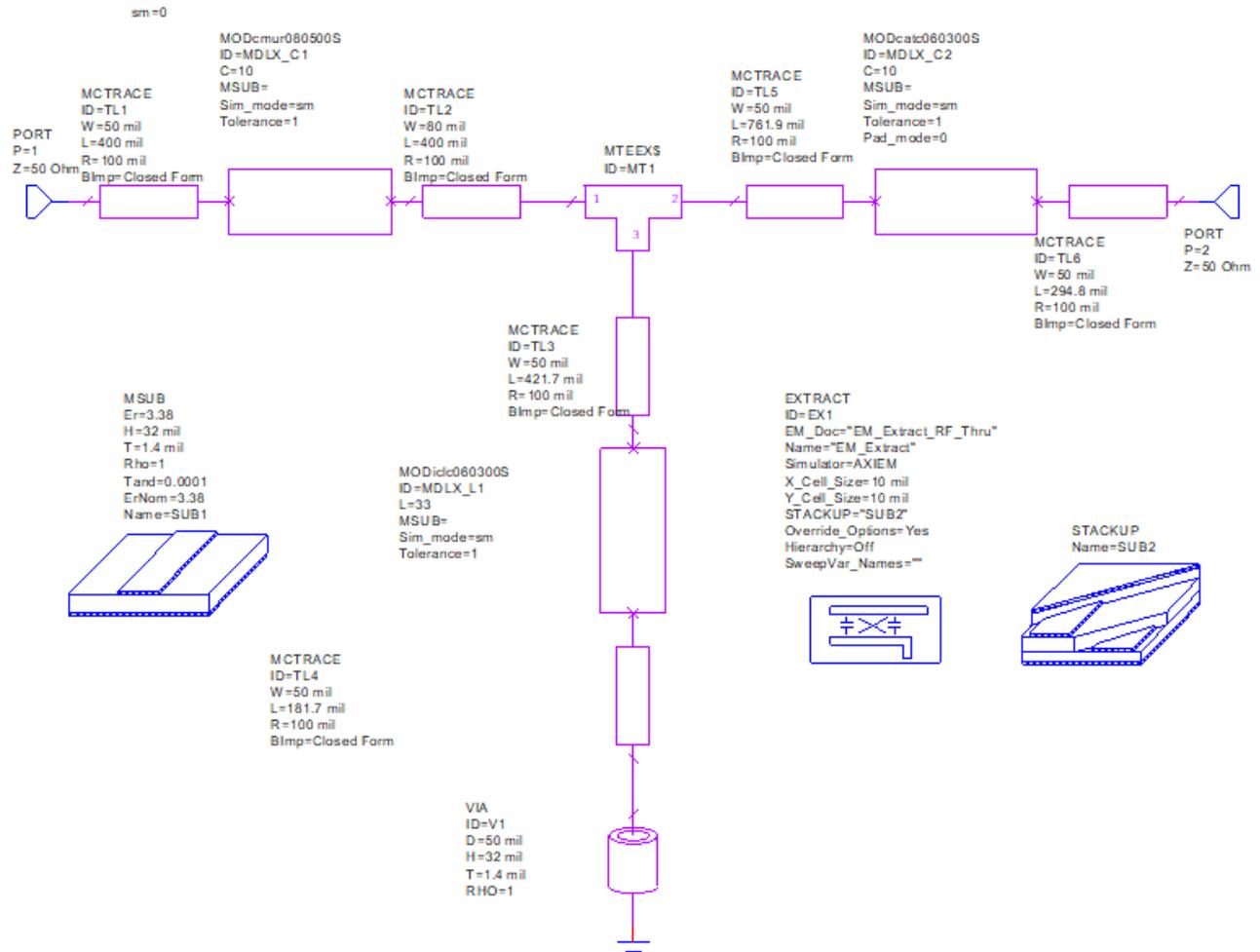
The graphs "Bias S11" and "Bias S21" show the effects of using more accurate simulation techniques. The Modelithics parts provide the designer with a more detailed understanding of his circuit. As the designer explores the circuit in more detail, it is obvious that the routed thru portion of the bias network is not precisely modeled by the MCTRACE, because of the internal meandering of the MCTRACE, and EM analysis is desired.

The combination of ease of use, Modelithics' library parts, and EM analysis provides a very fast and effective way to get highly accurate information and a detailed understanding of the circuit.

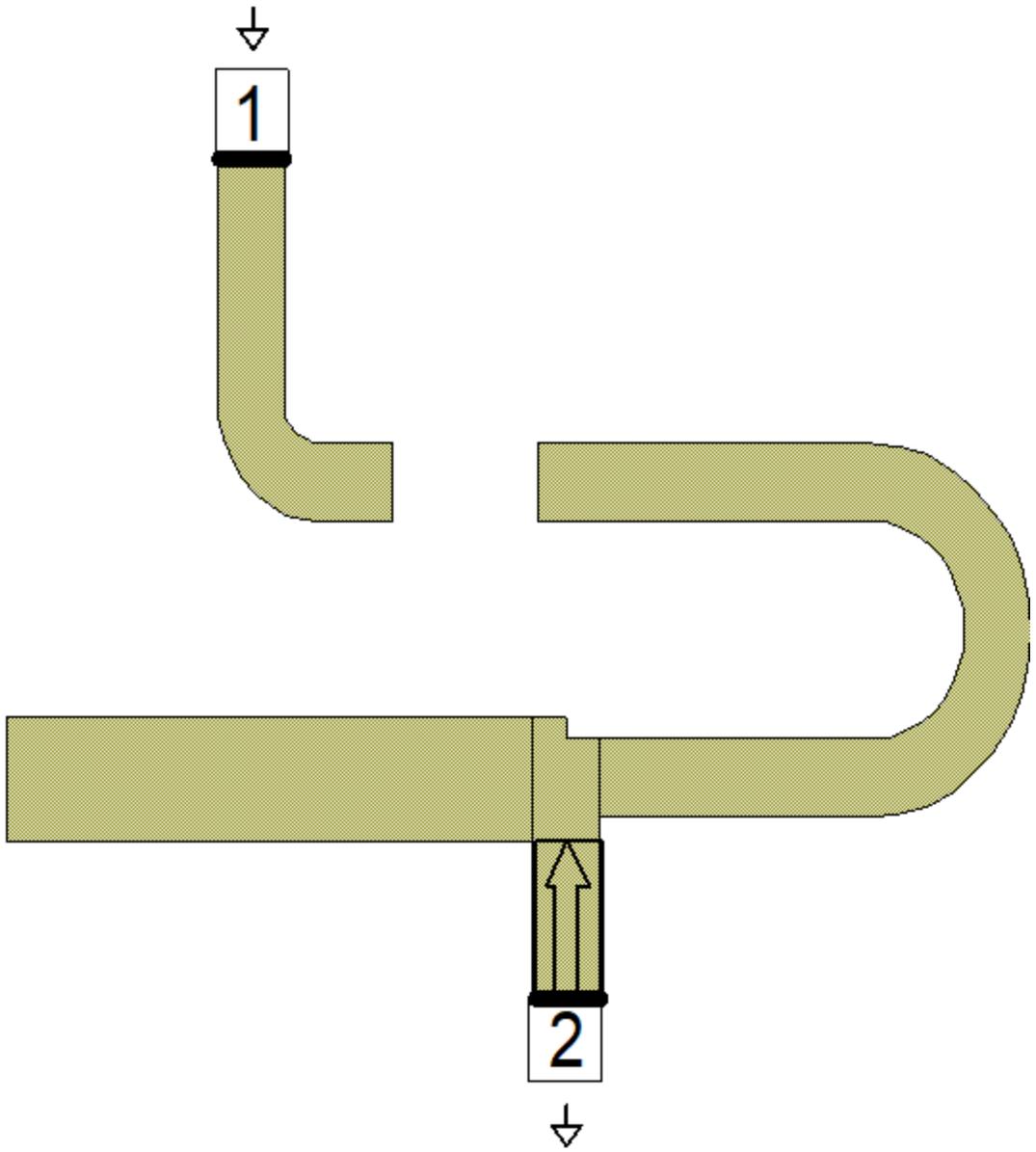
Schematic - Bias_Circuit_Based



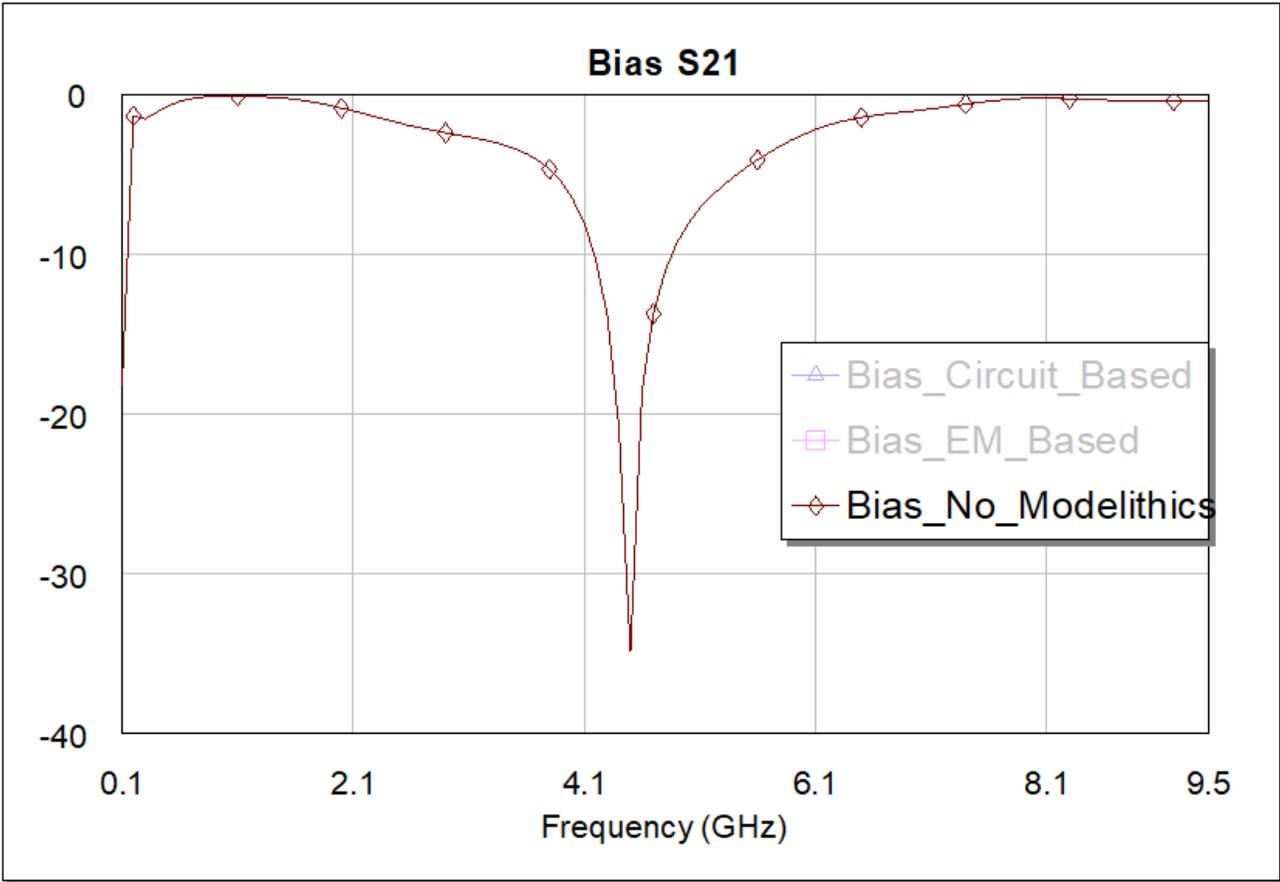
Schematic - Bias_EM_Based



EM Structure - EM_Extract_RF_Thru



Graph - Bias S21



Graph - Bias S11

