Modelithics_Bias_TEE

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Design Notes

Bias Tee Example

This example compares bias tee-type circuits that use standard "full parasitic" models from the Modelithics CLR Library to a circuit that uses ideal models. The ideal model response is obtained by setting the Sim_mode parameter for the models to 1. This examples also demonstrates the uses of part value arrays (found in the resources folder of the XML library) for discrete value optimization.

PDK

You must first install the Modelithics Select Library to properly simulate this example. You can obtain this library from AWR downloads page under "Vendor Libraries" tab.

Overview

Referring to the basic topology of the schematic Example_BIAS_TEE_1 included in this project, an ideal bias tee has the following properties: Port 1 is DC isolated, Port 3 is RF isolated, and an RF signal applied to Port 1 and a DC signal applied to Port 3 are perfectly combined at Port 2. Therefore, in the RF operating frequency range of an ideal bias tee, S11 is zero, S21 is one, and S31 is zero.

A commercial bias tee is typically designed using high value, broadband blocking capacitors along with broadband RF chokes (the inductor). These component types have not been used in this example, as the intent is not to present high performance bias tee design. Rather, the goal is to demonstrate differences in resulting parameter values for circuits that are optimized using accurate (full parasitic) substrate scalable models, and those using ideal LC models. A series C - shunt L configuration is one way to show the differences, which can be significant even for this simple two-element configuration.

For this example, an optimization goal was set up to obtain S11 less than -20 dB from 0.75 - 1.5 GHz. Discrete part value optimization was performed using the Pointer - Robust Optimization algorithm.

Optimization was first performed for the circuits shown in Example_BIAS_TEE_1 (full parasitic models) and Example_BIAS_TEE_2 (ideal models). The resulting element values are as follows:

Using parasitic models: C=47 pF and L=33 nH

Using ideal models: C=15 pF and L=120 nH

Simulation

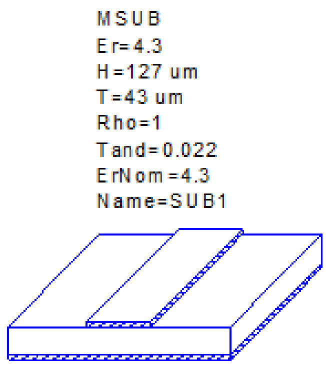
The frequency response for each circuit is shown in the Example_BIAS_TEE_DEMO_1_OPT graph.

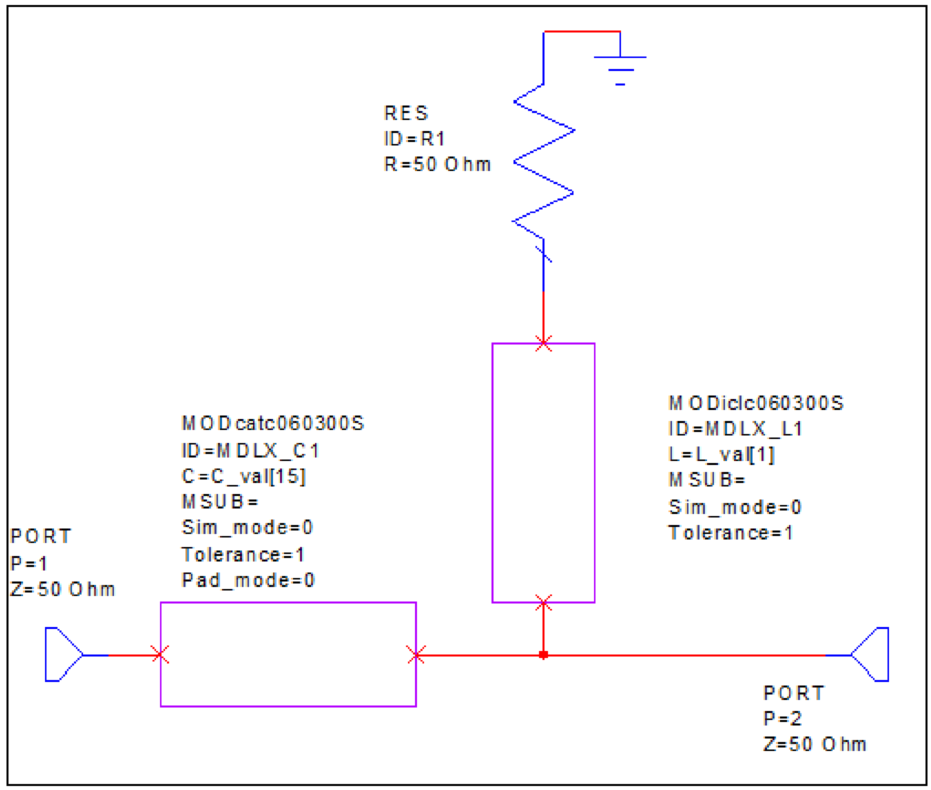
In the Example_BIAS_TEE_3 schematic, a circuit is shown that uses parasitic models with the element values assigned to those from the ideal model schematic. A comparison between the response of the ideal and parasitic model schematics is shown in the Example_BIAS_TEE_DEMO_1 graph. The results demonstrate that the bias tee circuit---when using the accurate full parasitic models and the element values from the ideal schematic---does not meet the required performance specification. In other words, the bias tee would not operate as expected if designed using ideal element characteristics.

Schematic - Example_BIAS_TEE_1

Discrete part values for the Select version of the IND_CLC_0603_001 model:
L_val={33,36,39,43,47,51,56,68,72,82,100,110,120,150,180,200,210,220,250,270}

Discrete part values for the Select version of the CAP_ATC_0603_001 model:
C_val={10,11,12,15,18,20,22,24,27,30,33,36,39,43,47,51,56,62,68,75,82,91,100}





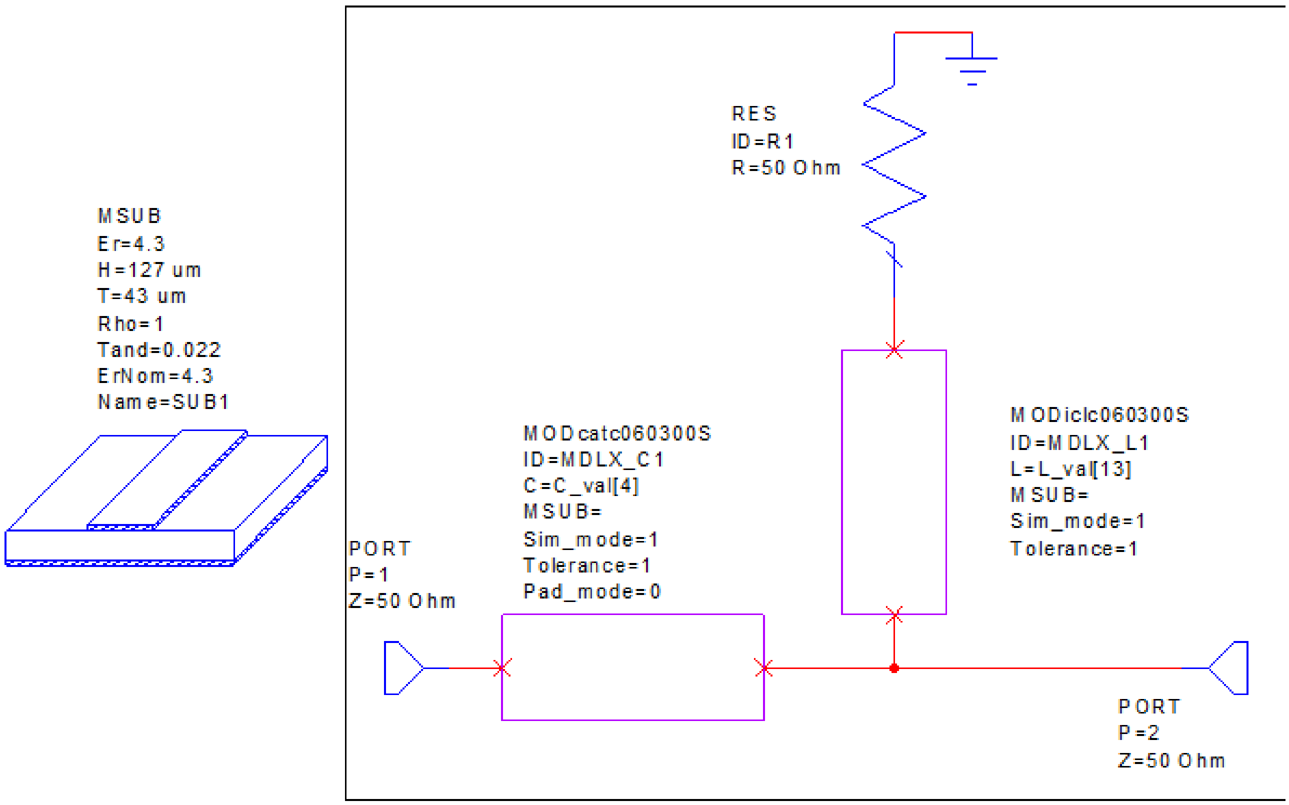
Circuit after discrete part value optimization using parasitic models.

(NOTE: Sim_mode = 0 for both models.)

Schematic - Example_BIAS_TEE_2

Discrete part values for the Select version of the IND_CLC_0603_001 model:
L_val={33,36,39,43,47,51,56,68,72,82,100,110,120,150,180,200,210,220,250,270}

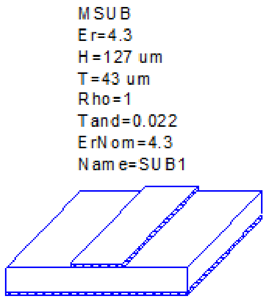
Discrete part values for the Select version of the CAP_ATC_0603_001 model:
C_val={10,11,12,15,18,20,22,24,27,30,33,36,39,43,47,51,56,62,68,75,82,91,100}



Circuit after discrete part value optimization using ideal models.

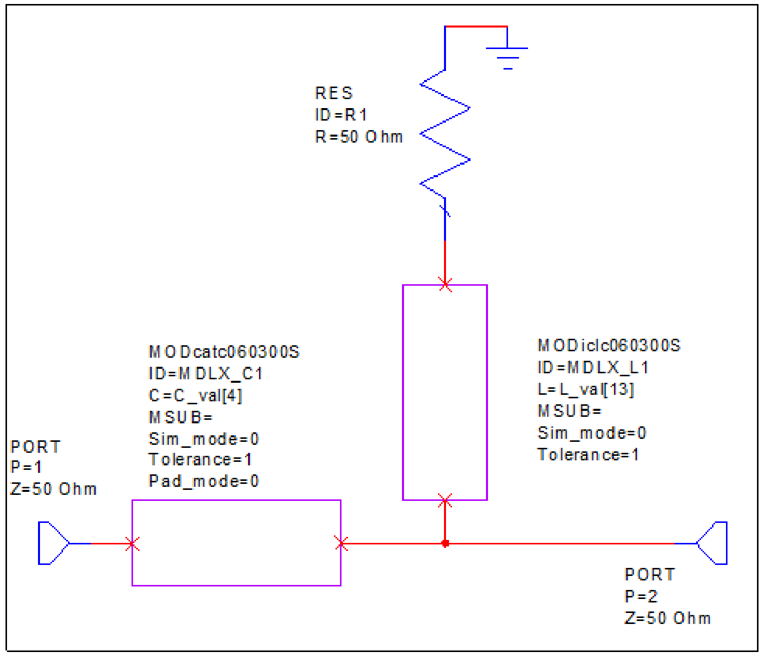
(NOTE: Sim mode = 1 for both models.)

Schematic - Examples_BIAS_TEE_3



Discrete part values for the Select version of the IND_CLC_0603_001 model:
L_val={33,36,39,43,47,51,56,68,72,82,100,110,120,150,180,200,210,220,250,270}

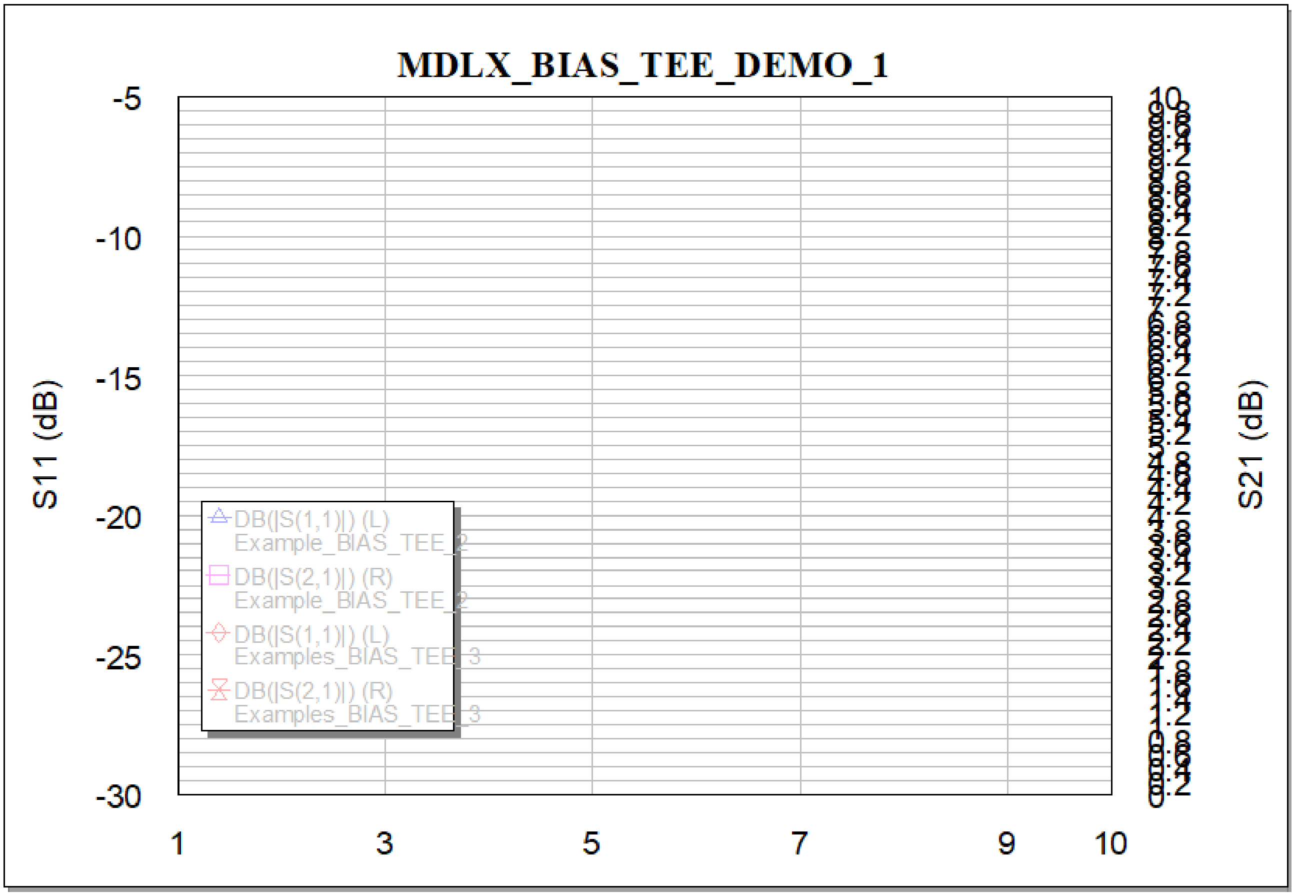
Discrete part values for the Select version of the CAP_ATC_0603_001 model:
C_val={10,11,12,15,18,20,22,24,27,30,33,36,39,43,47,51,56,62,68,75,82,91,100}



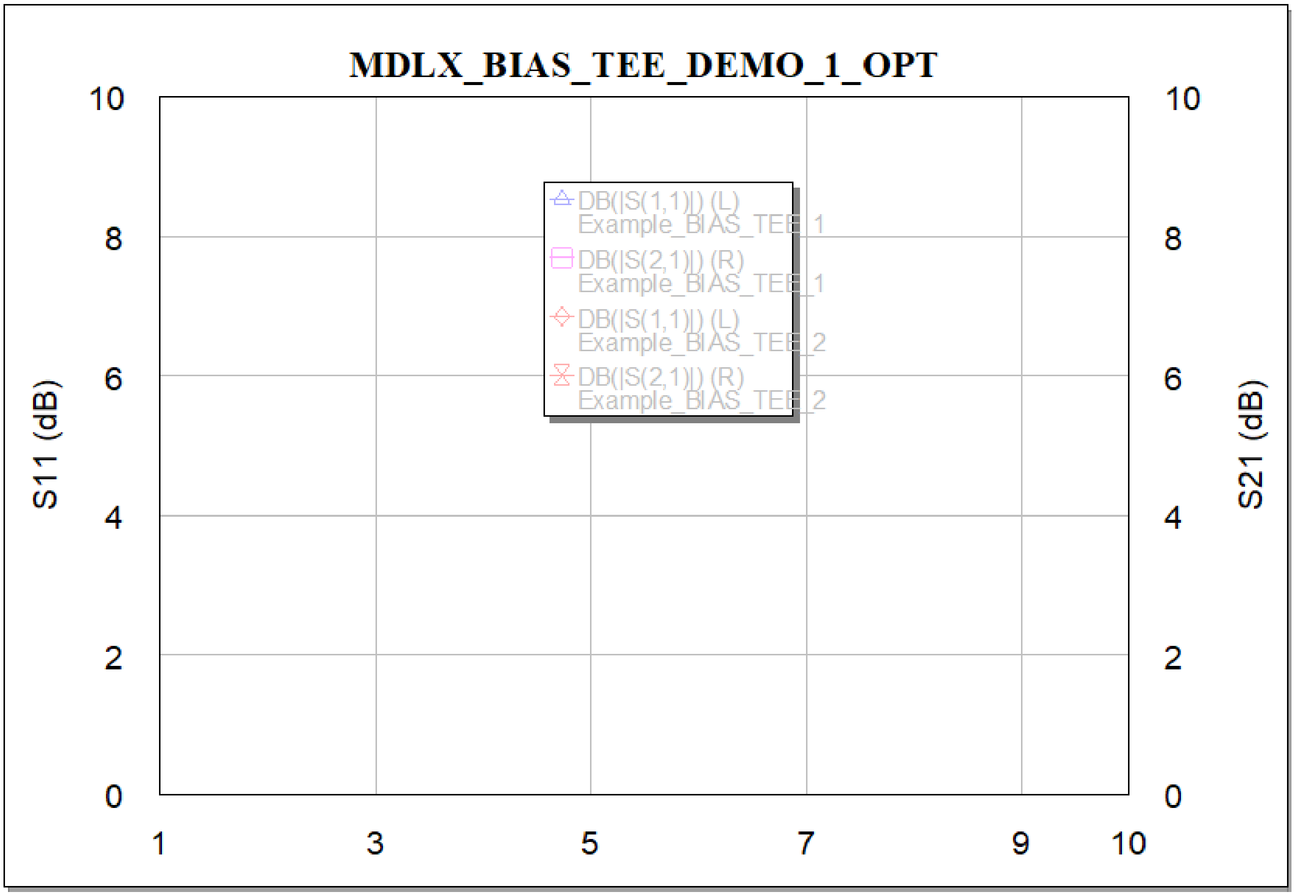
Circuit using parasitic models with values from optimized ideal model circuit.

(NOTE: Sim mode = 0 for both models.)

Graph - MDLX_BIAS_TEE_DEMO_1



Graph - MDLX_BIAS_TEE_DEMO_1_OPT



MDLX_BIAS_TEE_DEMO_1_OPT
10
8
6
4
2
0
S11 (dB)
10
8
6
4
2
0
S21 (dB)
1
3
5
7
9
10
DB(|S(1,1)|) (L)
Example_BIAS_TEE_1
DB(|S(2,1)|) (R)
Example_BIAS_TEE_1
DB(|S(1,1)|) (L)
Example_BIAS_TEE_2
DB(|S(2,1)|) (R)
Example_BIAS_TEE_2