Distributed_Amplifier

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Design Notes

Distributed Amplifier

This example demonstrates a MMIC design of a distributed amplifier with a flat gain of about 12dB from about 2GHz to 10GHz. It is an extension of the original Distributed Amplifier example to now include Parametric Layout.   The circuit is simulated using both ACE (Automatic Circuit Extraction), and AXIEM with AFS band limit, geometry simplification rules, and auto ports.

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This project does not include the datasets, therefore simulating this project with EXTRACT blocks enabled will take approximately 40 minutes. However this example is available with datasets at : https://awrcorp.com/download/faq/english/examples/Distributed_Amplifier.aspx

Parametric Layout, Axiem and ACE

In addition, we have included the application of the parametric layout feature. This feature allows the designer to pass down any parameter through hierarchy to subcircuits which include layout. Each of the gate and drain lines creating the distributed amplifier have been represented by the same parametric subcircuit with associated layout called "Trombone Parameterized". However, since different layout parameters are passed to each individual subcircuit, they all unique. The layout will automatically update to reflect changes to each of those parameters.

ACE

Also, demonstrated in this example is Extraction using ACE (Automatic Circuit Extraction). You must have a license file that supports ACE for this to work. An **EXTRACT** block is included in the schematic titled Distributed_Amplifier_Testbench_ACE. The **EXTRACT** block is disabled. Run the simulation with the Extract block disabled. On the Graph "Gain and S11 and S22_ACE", choose **Graph>Freeze Traces**. Now, enable the **EXTRACT** block by right clicking the Extract block and choosing Toggle Enable. Re-run the simulation. Notice several things:

1. A new EM structured named **ACE_Extract_Doc** was automatically created. If you Right Mouse Click on this EM document, select **Add Annotation,** select **ERC** from the **Measurement** Type section, select **EXT_CKT3D**, and select **OK** you can view the elements extracted in a 3D view of the EM document.

2. The bandwidth of the distributed amplifier has actually increased by a substantial amount. In the case, the simulated coupling in each of the trombone sections has worked in favor of larger of bandwidth. With parametric layout and ACE together, the design process for many circuits can be much more efficient.

3. Notice the **EXTRACT** block has a parameter named **Hierarchy** that is set to **On.** This tells the simulator to perform the extraction at the hierarchical level where the block is and use those extraction results when used at any higher level. So in this case, the extraction will affect both test benches in this project. If this parameter were set to **Off**, you would not see any difference due to ACE extraction.
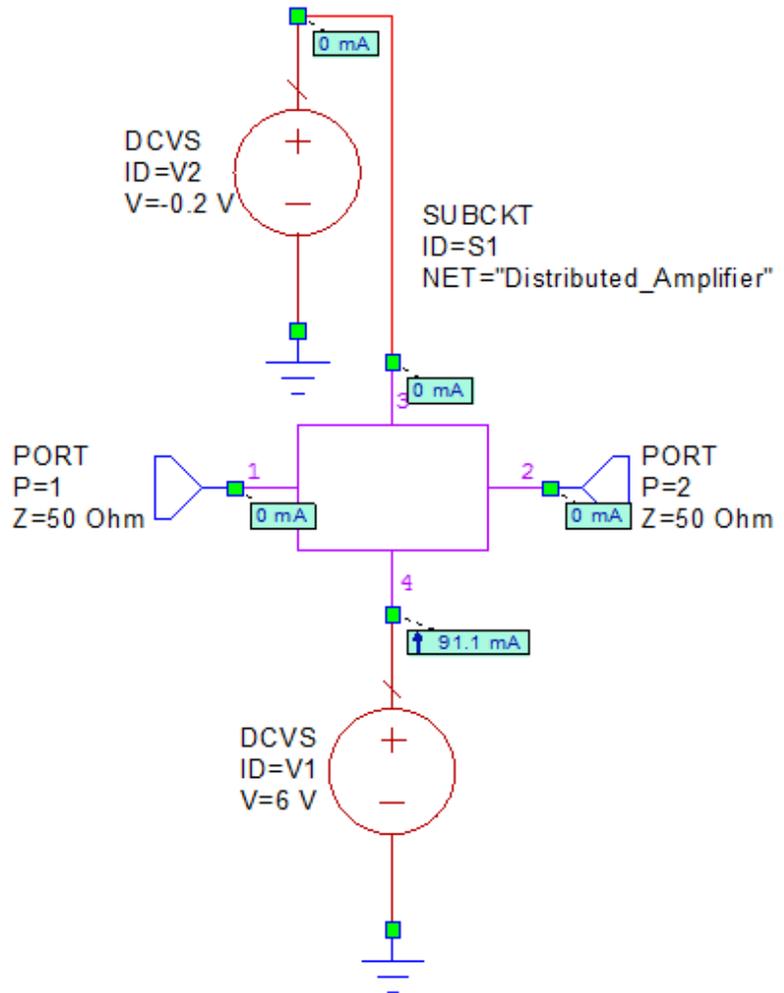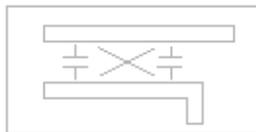
AXIEM

Also, demonstrated in this example is Extraction using AXIEM. You must have a license file that supports AXIEM for this to work. Similarly, the **EXTRACT** block in the schematic titled Distributed_Amplifier_Testbench_Axiem is disabled. Enabling this block will create a new structure called **Axiem_Extract_Doc** which will EM simulate the structure. The AXIEM structure is set to use AFS band limit from 0.5 GHz to 10 GHz. AFS will not be used outside that band. Geometry simplification rules are written in the STACKUP to simplify the plated line geometry for more efficient meshing. All the ports in the extracted AXIEM structure are auto ports. Right Click select **Axiem_Extract_Doc > Preview Geometry** to see the simplified geometry and port settings determined by auto ports.

Schematic - Distributed_Amplifier_Testbench_ACE
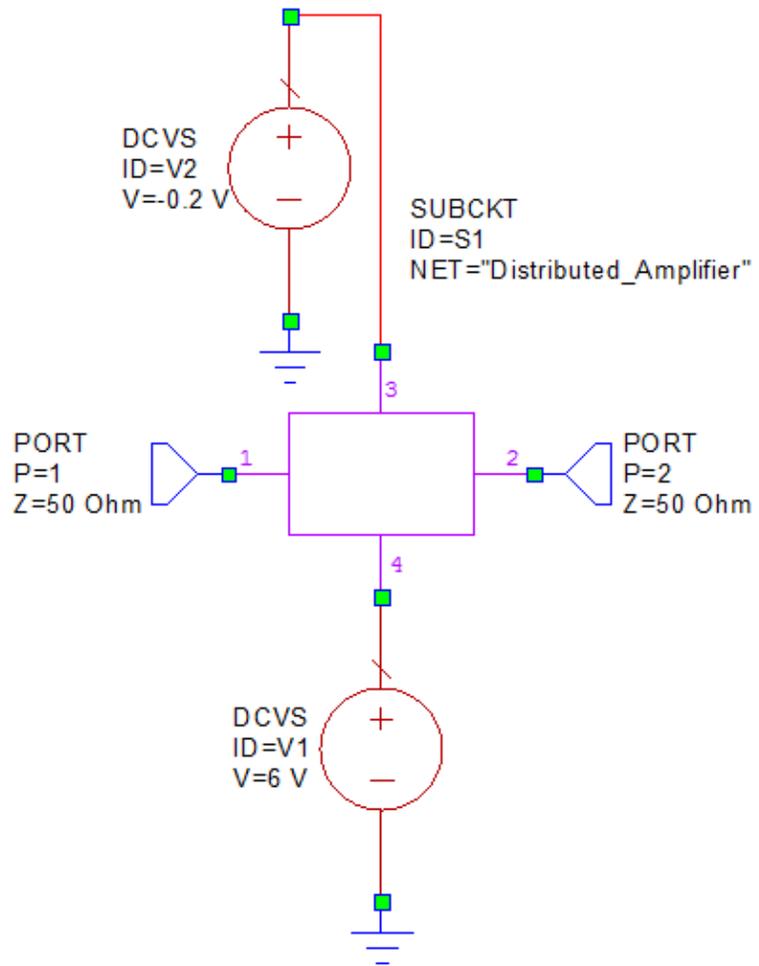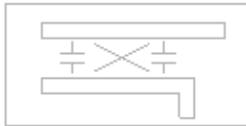
Distributed Amplifier Testbench - ACE

EXTRACT
ID=EX1
EM_Doc="ACE_Extract_Doc"
Name="EM_Extract"
Simulator=ACE
X_Cell_Size=1 um
Y_Cell_Size=1 um
STACKUP="SUB"
Override_Options=Yes
Hierarchy=On
SweepVar_Names=""

DCVS
ID=V2
V=-0.2 V

0 mA

SUBCKT
ID=S1
NET="Distributed_Amplifier"

0 mA

PORT
P=1
Z=50 Ohm

1

0 mA

2

PORT
P=2
0 mA   Z=50 Ohm

4

91.1 mA

DCVS
ID=V1
V=6 V
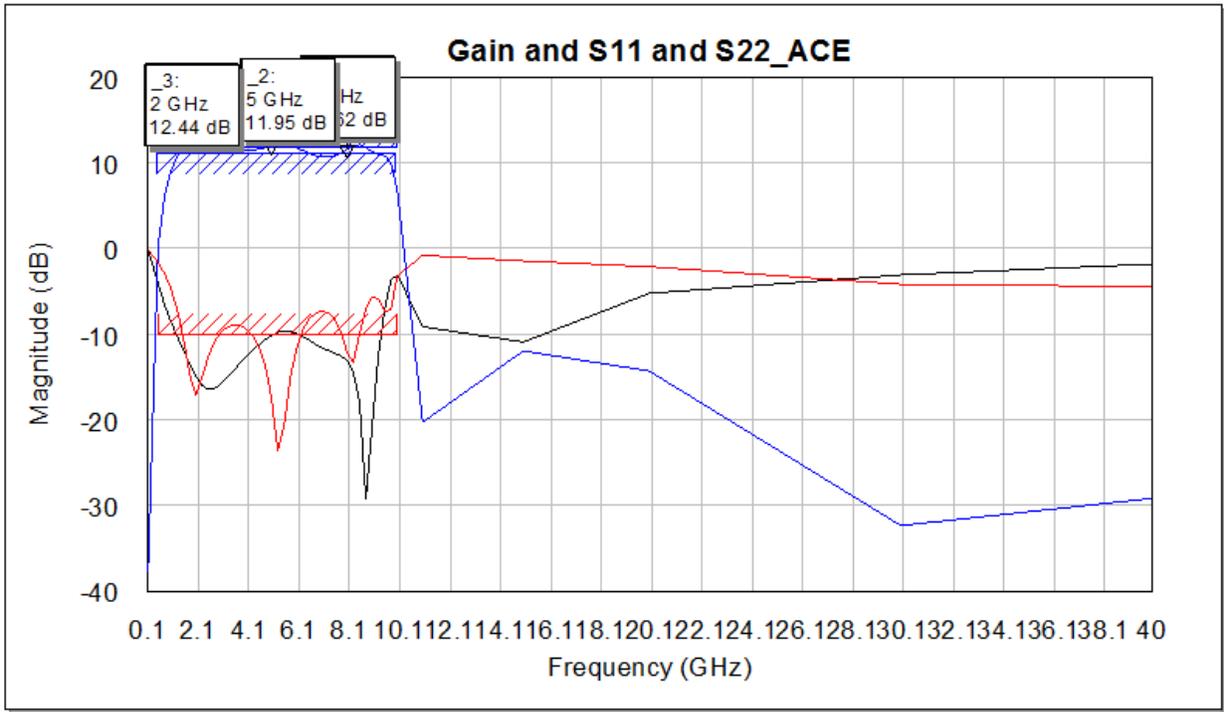
Schematic - Distributed_Amplifier_Testbench_Axiem

Distributed Amplifier Testbench - Axiem

EXTRACT
ID=EX1
EM_Doc="AXIEM_Extract_Doc"
Name="EM_Extract"
Simulator=AXIEM
X_Cell_Size=2.5 um
Y_Cell_Size=2.5 um
STACKUP="SUB"
Override_Options=Yes
Hierarchy=On
SweepVar_Names=""

DCVS
ID=V2
V=-0.2 V

SUBCKT
ID=S1
NET="Distributed_Amplifier"

PORT
P=1
Z=50 Ohm

1

3

2

PORT
P=2
Z=50 Ohm

4

DCVS
ID=V1
V=6 V

Graph - Gain and S11 and S22_ACE

Graph - Gain and S11 and S22_Axiem