EM_PCB_Via_Merging

Where To Find This Example

Select **Help > Open Examples...** from the menus and type either the example name listed above or one of the keywords below.

Or in Version 14 or higher you can open the project directly from this page using this button. Make sure to select the **Enable Guided Help** before clicking this button.

Open Install Example

Design Notes

Axiem EM Solver PCB VIA Pre-Processing

This project demonstrates the capabilities of AXIEM rules based geometry simplification. In this case a sample 4 layers PCB is shown and it is based on the generic AWR_Module process.

Overview

In this example, arrays of PCB vias are merged together prior to being meshed in order to cut down on the number of unknowns to be solved.

Vias in close proximity are detected and merged for meshing based on user's control and preference. The layout of all shapes are preserved, and only the geometry being simulated by AXIEM is simplified. The user can freely choose to turn ON or OFF the shape pre-processing capabilities.

From the layout view of the schematic, the user is free to add and delete vias (by copying and pasting), also change the routing of the MCTRACE element. The user is free to experiment with different vias distribution and the effects of using shape pre-processing in AXIEM EM Solver.

Schematic of Extracted Layout

The schematic "Via_on_Plane" utilizes the MCTRACE element. In schematic layout, the ground plane is drawn on a positive layer. The combination of the MCTRACE line type, defined with a negative layer, ground plane defined with a positive layer produces cutouts in the ground plane. For more details on the Positive and Negative layers in AWR's layout, refer to the User's Guide's chapter on layout. Or search our Knowledge Base for the keyword "Layers".

Vias are also added to the layout view in various distributions around the signal line and throughout the plane acting as ground. To include a shape in EM Extraction, right-click select the shape in the layout view, and then select **Shape Properties > Layout Tab.** Then check the option to enable **EM Extraction.** Refer to AWR Documentation for more details on extraction.

Geometry Simplification and Extraction to Axiem

To add the shapes from the schematic layout view to the AXIEM EM structure, right click on the Extract block in the "Via_on_Plane" schematic and select **Add Extraction.** For more information on Extraction consult Simulation and Analysis Guide and our Knowledge Base.

The extract block references a STACKUP named "Thin_Metal" that is located in the Global Definitions. Double click on this STACKUP and go to the **Rules** tab to see the geometry simplification rules. There are comments above each rule explaining what they do.

Viewing Simplified Geometry

After you have created the EM document there are several ways to see the simplified geometry. You can right click on the EM document and select **Preview Geometry** to see a new view showing the processed geometry. You can also mesh the structure to see how the mesh will look for the structure. Open a 3D view of the structure (with the 2D layout active, select **View EM 3D Layout**) and then click the **Show 3D Mesh** button from the toolbars.

You can see the effect each simplification rule will have on the size of problem to solve. The easiest way to do this is to comment out individual rules in the global STACKUP element, then right click on the EXTRACT block in the schematic and select **Add Extraction**. Finally, mesh the newly updated EM structure. After meshing is complete double click on the **Information** node under the EM structure in the project tree to see the listing of the number of unknowns.

The approximate problem size is listed below with the specific rules enabled:

No Rules = 20,500

After Via Pad Removal = 19,500

After Via Merging = 5,250

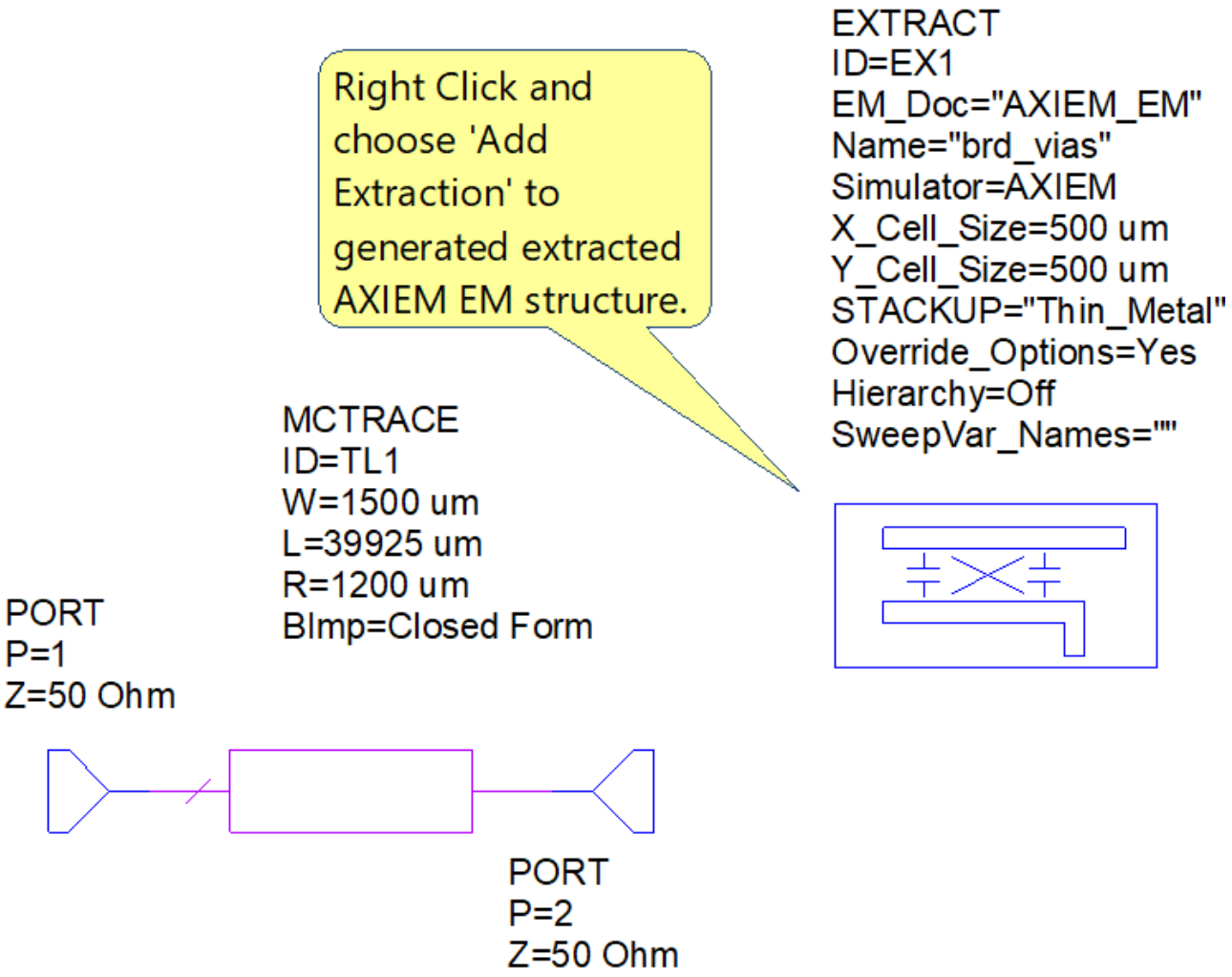
After Decimation = 2,500

As you can see the rules have made an order of magnitude reduction in the problem that must be solved. The via merging rules will take some time to complete. The reduction in the problem size is well worth this upfront time.

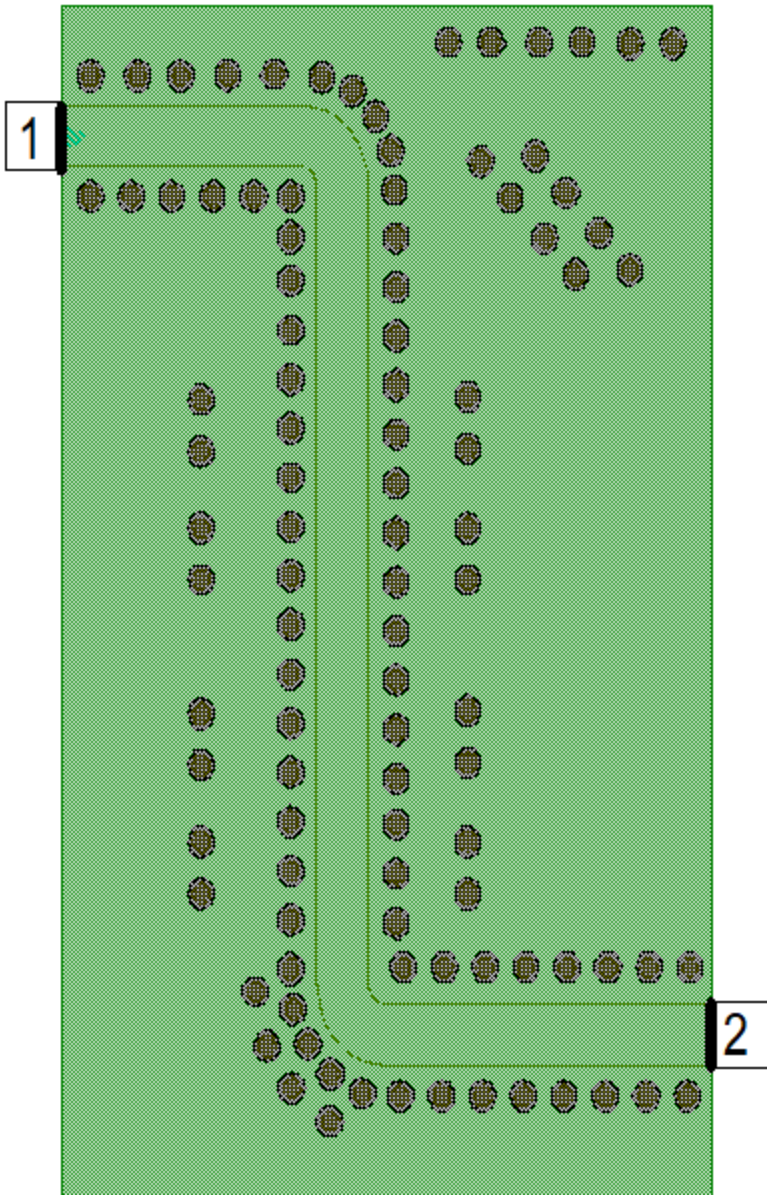
Simulating Results

The project includes a graph that shows the simulation results of the MCTRACE element from the schematic. Simulate with the Extract block enabled and disabled to view differences between the EM simulated results and circuit model results. The MCTRACE circuit model assumes an infinite ground plane without any ground return on its side. In the case of extraction to EM, the ground return from vias surrounding the MCTRACE is also modeled.

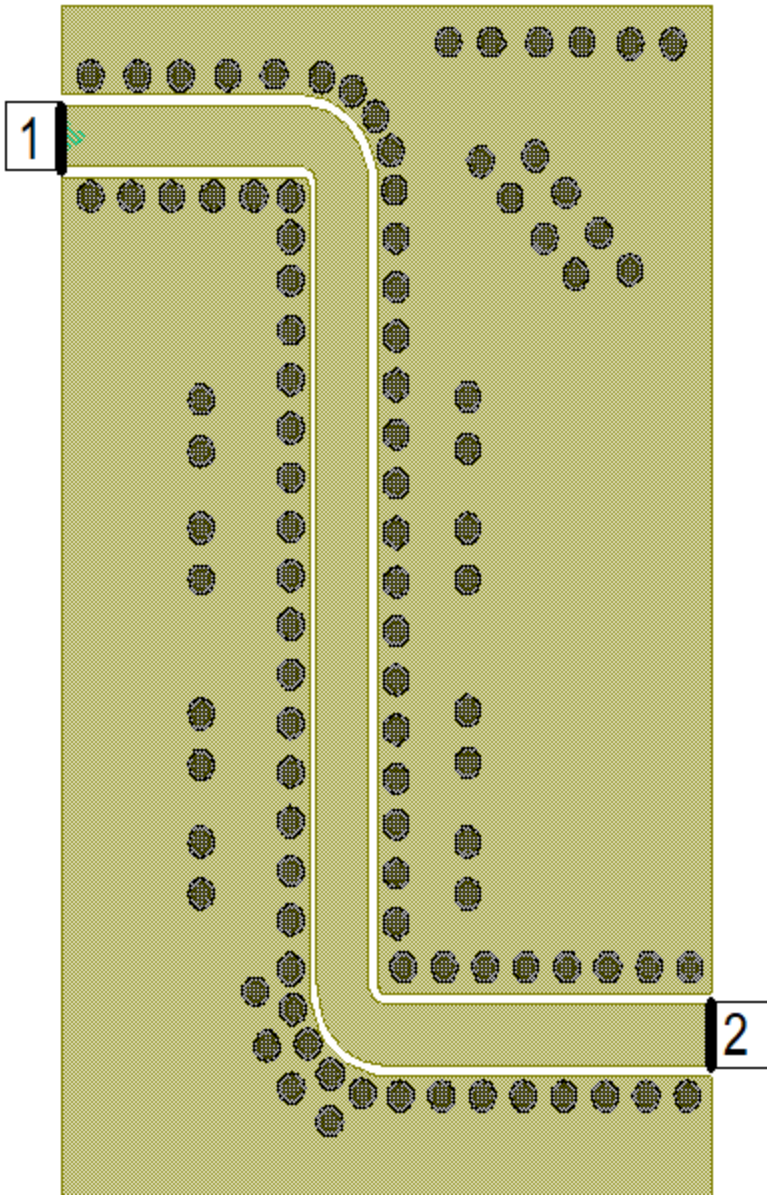
Schematic - Via_on_Plane



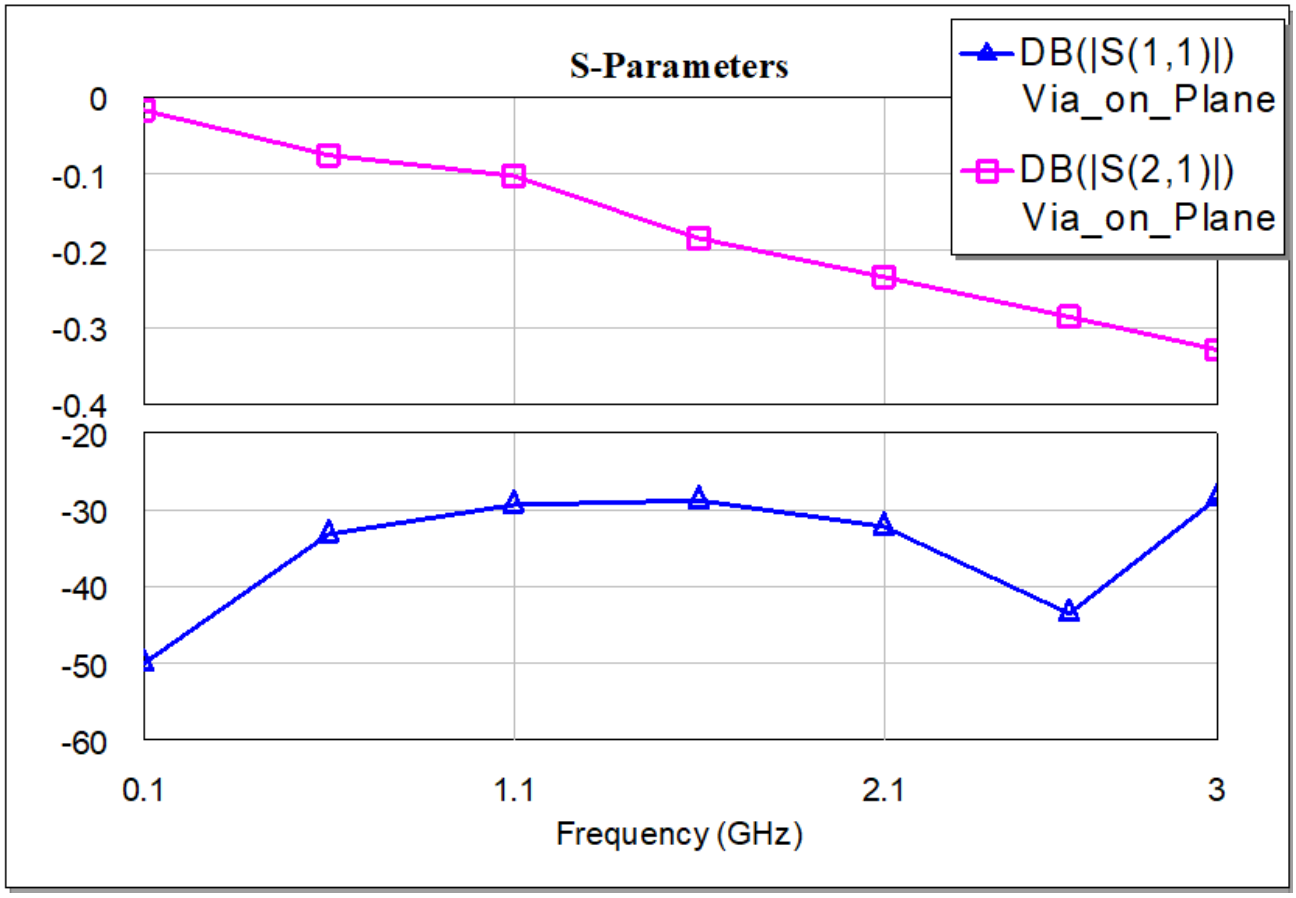
Schematic Layout - Via_on_Plane



EM Structure - AXIEM_EM



Graph - S-Parameters


S-Parameters
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DB(|S(2,1)|) Via_on_Plane
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-0.1
-0.2
-0.3
-0.4
-20
-30
-40
-50
-60
0.1
1.1
2.1
3
Frequency (GHz)