Infineon_VCO

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Design Notes

Infineon Voltage Controlled Oscillator

This example demonstrates the simulation of a voltage controlled (VCO) oscillator. The design is taken from an application note written by engineers at Infineon titled *W-CDMA 2.3 GHz VCO using BFR360F and BBY58-02V*. The design is outlined in the PDF file "Appli061_WCDMA_VCO.pdf" which can be found in the same directory as this project (Help > Show Files/Directories > Examples).

Overview

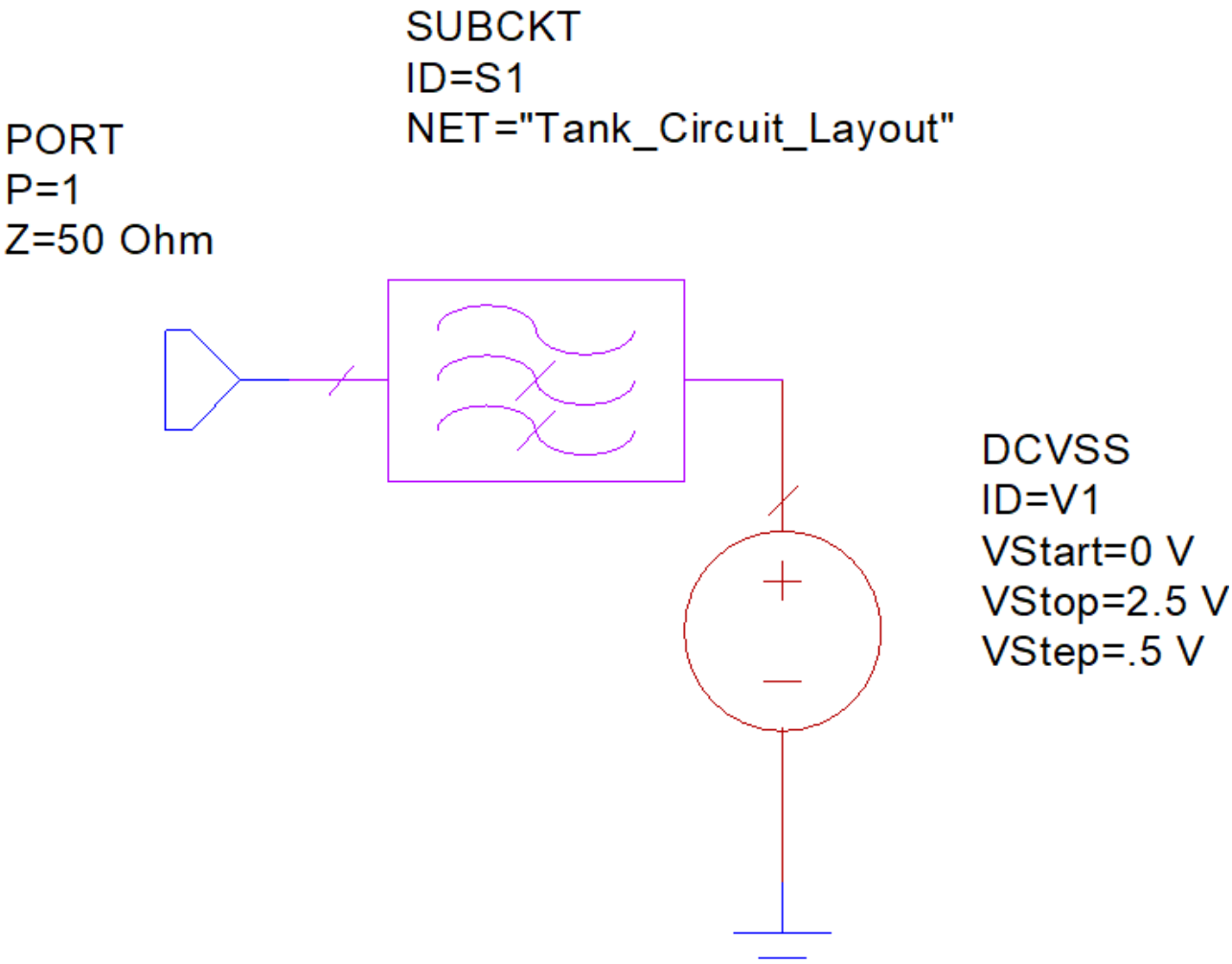
This example shows the design of a VCO oscillator. It uses a varactor diode for the voltage control in the tank circuit, and a bipolar transistor negative resistance source. The project is broken up into two main parts. First, a linear analysis of the oscillator is carried out in order to determine the correct oscillation frequency. The second part of the project performs a nonlinear analysis using the OSCAPROBE element. The frequency of oscillation is confirmed. A number of important oscillator performance characteristics are also calculated: output power spectrum, and phase noise. It can be seen how the oscillator's frequency can be changed with voltage.

The bipolar transistor is modeled using a GBJT chip model and includes package parasitics. The final model is shown in the schematic "BFR360F". The varactor diode with package parasitics is shown in the schematic "Varactor". A BBY53-02W diode was used in place of the BBY58-02V described in the application note. The parasitics are taken from a D353 sdiode chip model. The passive elements have different values than the application note, however, the results however are not extremely sensitive to them.

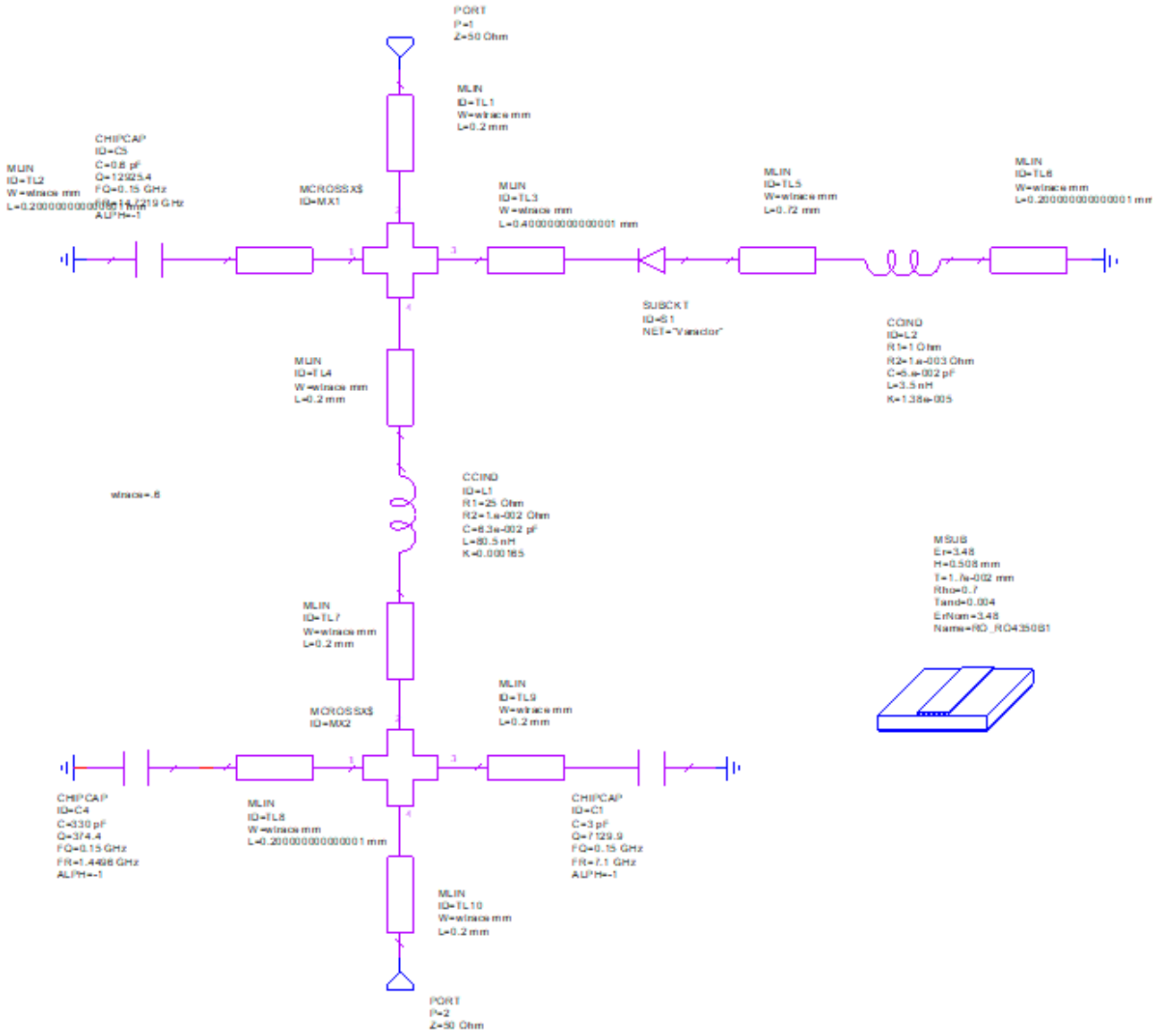
Part 1: Linear Simulation of the Oscillator

The circuit is first analyzed to determine it's approximate oscillation frequency using linear analysis concepts. The oscillator is designed using a negative resistance type of design where a tank circuit and a negative resistance source are attached to each other. The total admittance is then examined. When the conductance is negative and the susceptance is 0, the circuit will be in steady state oscillation.

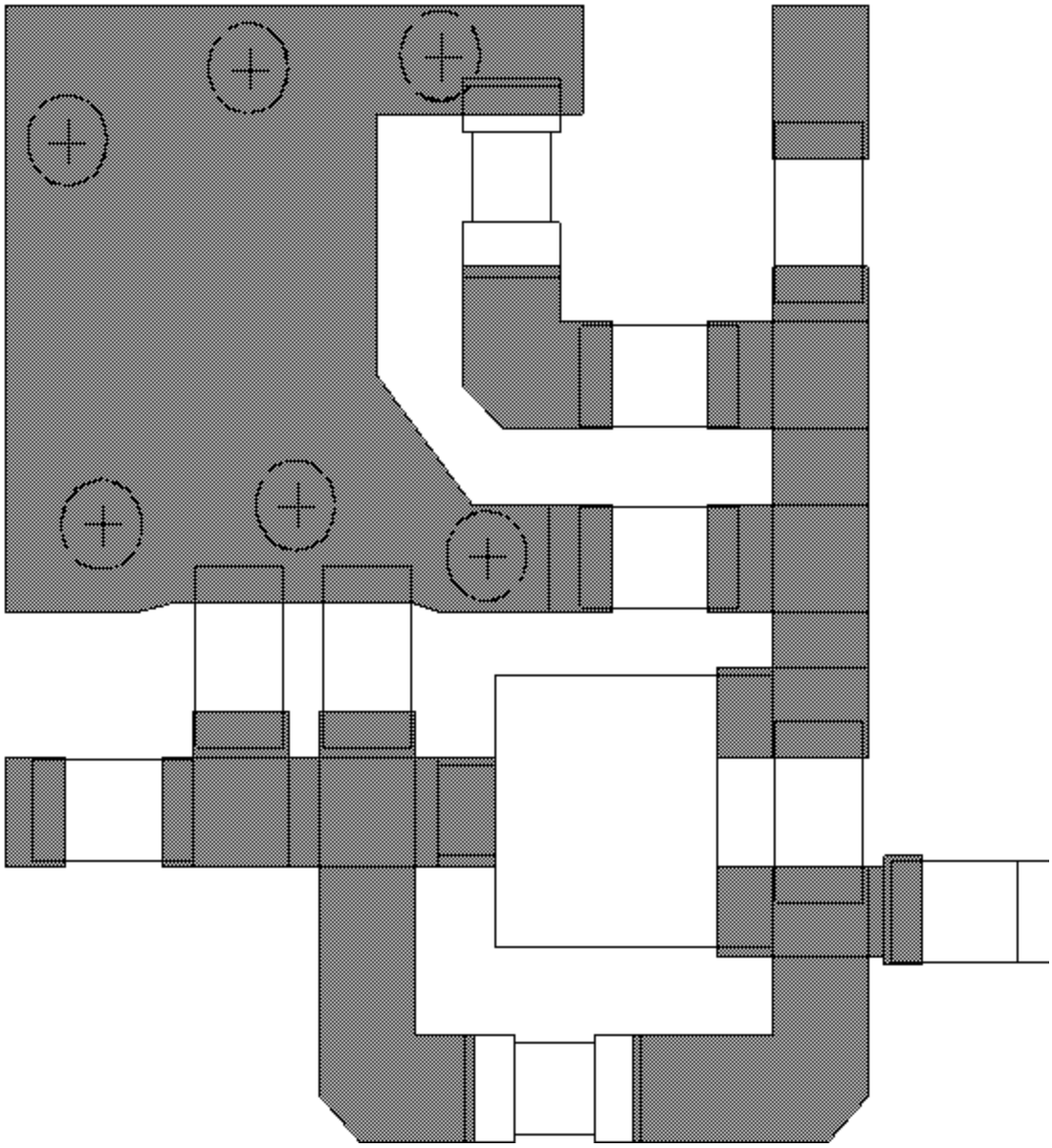
The schematic "1_Tank for Linear"

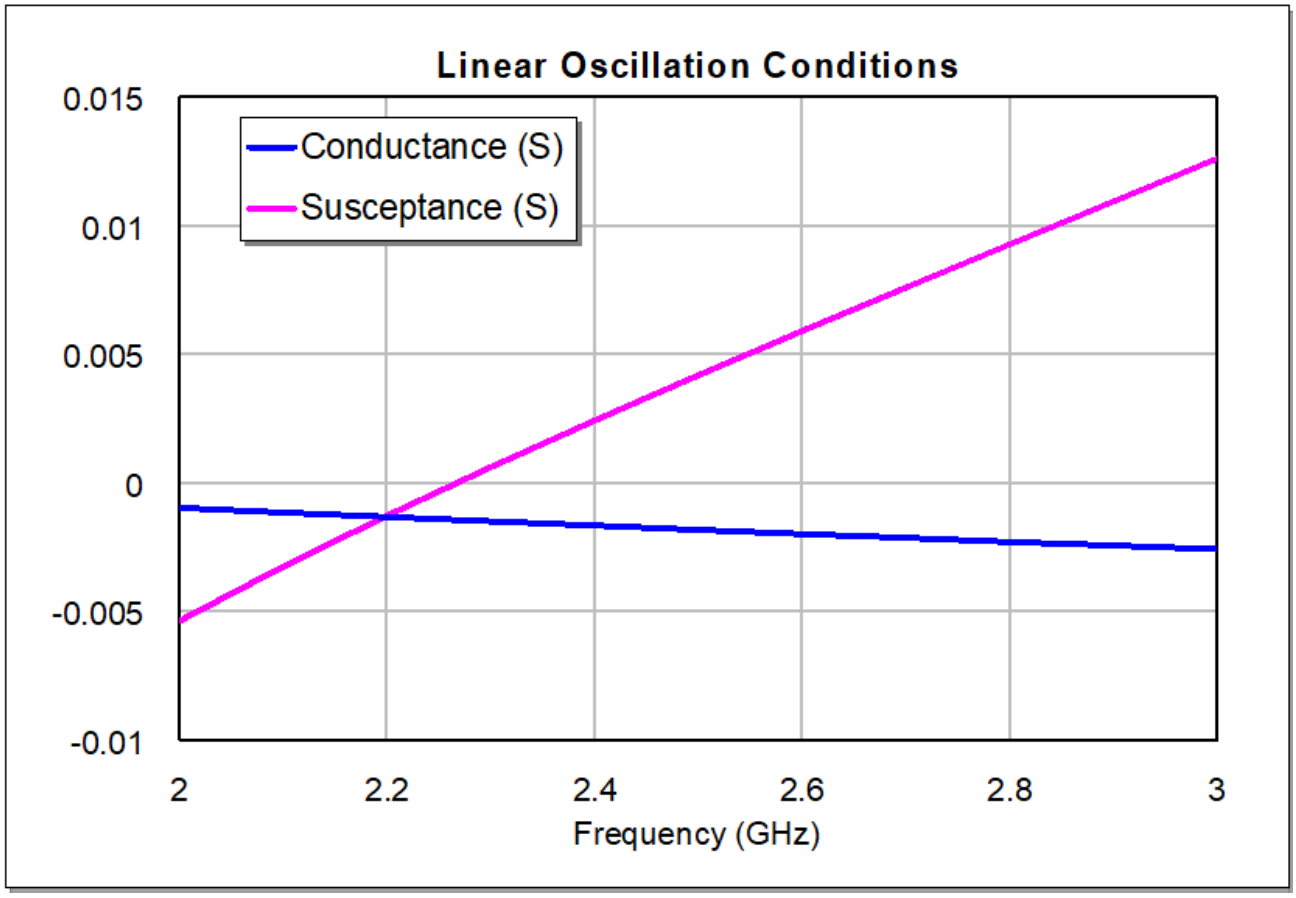


biases the varactor to the correct DC, anywhere from 0 to 2.5 Volts. The actual tank circuit is in "Tank Circuit Layout",



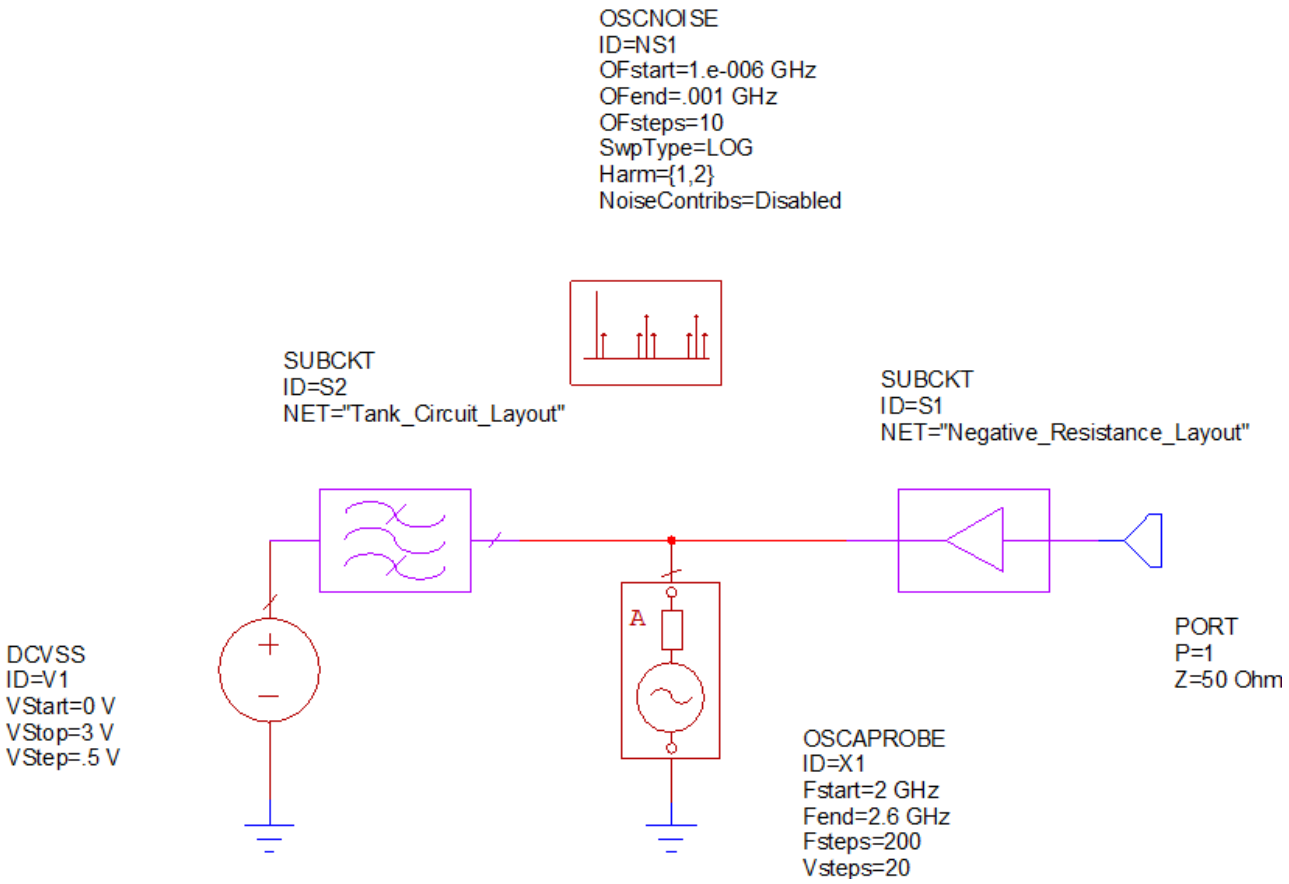
which has a schematic layout with the layout. The actual varactor model is in the schematic "Varactor". The negative resistance source is in the schematic "Negative Resistance Layout". It has an associated schematic layout.



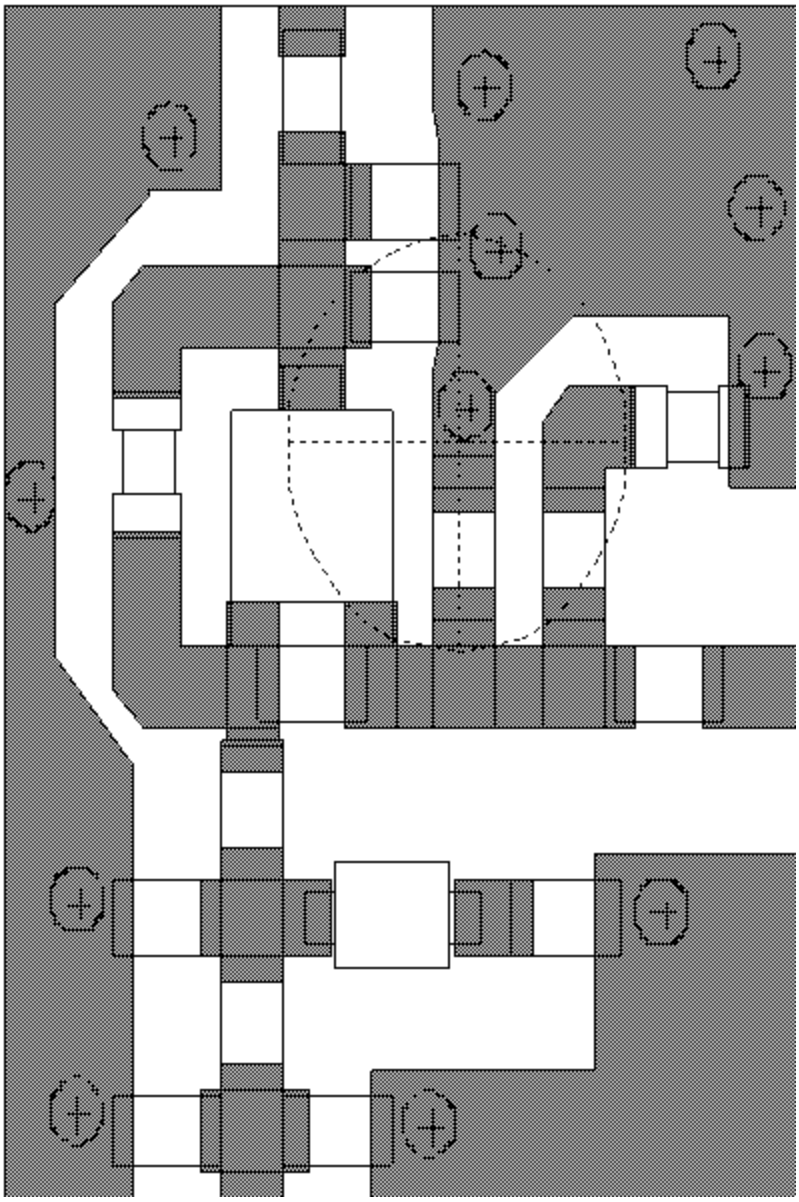


Graph "1_Linear Oscillation Conditions" shows the total admittance for the inputs of the tank circuit and the negative resistance source. This was accomplished by creating a variable **Y_total**, and graphing its real (conductance) and imaginary (susceptance) parts. **Y_total** is defined in the browser window "Output Equations" as the sum of the admittance of the tank circuit and the admittance of the negative resistance source. Oscillation should occur where the susceptance is 0, as the conductance is negative. The tuner can be used to tune over the DC voltage levels for biasing the varactor. Use the right "Vdc" parameter and watch the 0 crossing of the conductance change; i.e., the expected oscillation frequency is controlled by the varactor bias voltage.

Part 2: Nonlinear Simulation of the Oscillator

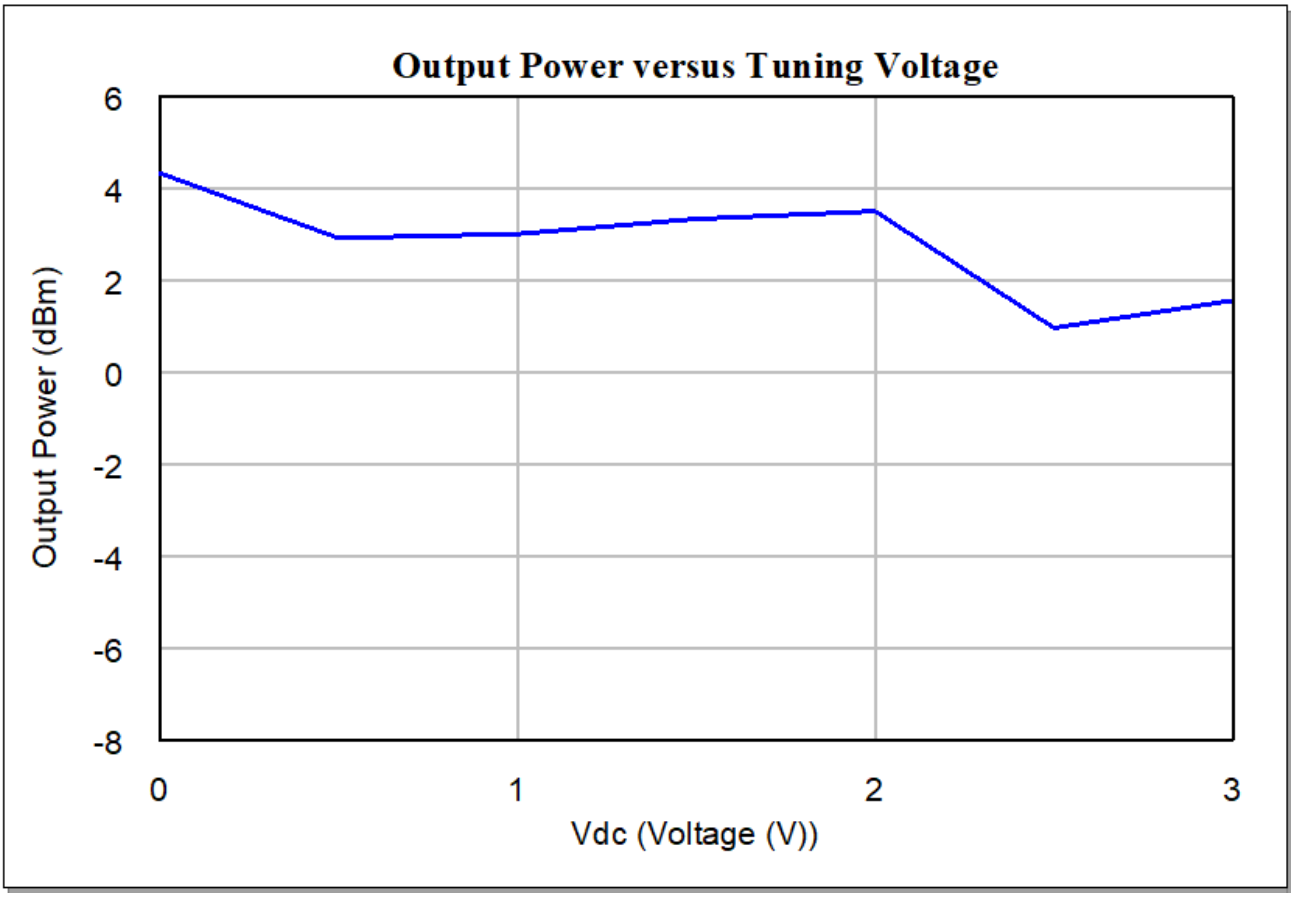


The second part of the analysis process is to simulate the oscillator under steady state, conditions. This is accomplished using harmonic balance and the OSCAPROBE element. The schematic "2_VCO" shows how the OSCAPROBE is used. The OSCAPROBE is inserted in parallel between the tank circuit and the negative resistance source. It is essentially a voltage source that sweeps over a range of frequencies and voltages until it finds a point where the net current flow through it is zero. At this point, the circuit is in steady state oscillation. The frequency range in this example covers the expected frequency of about 2.2 GHz, as predicted by the linear analysis. There is also an OSCNOISE element which controls the phase noise simulation. The DC voltage source to control the varactor bias can be swept from 0 to 3 V.

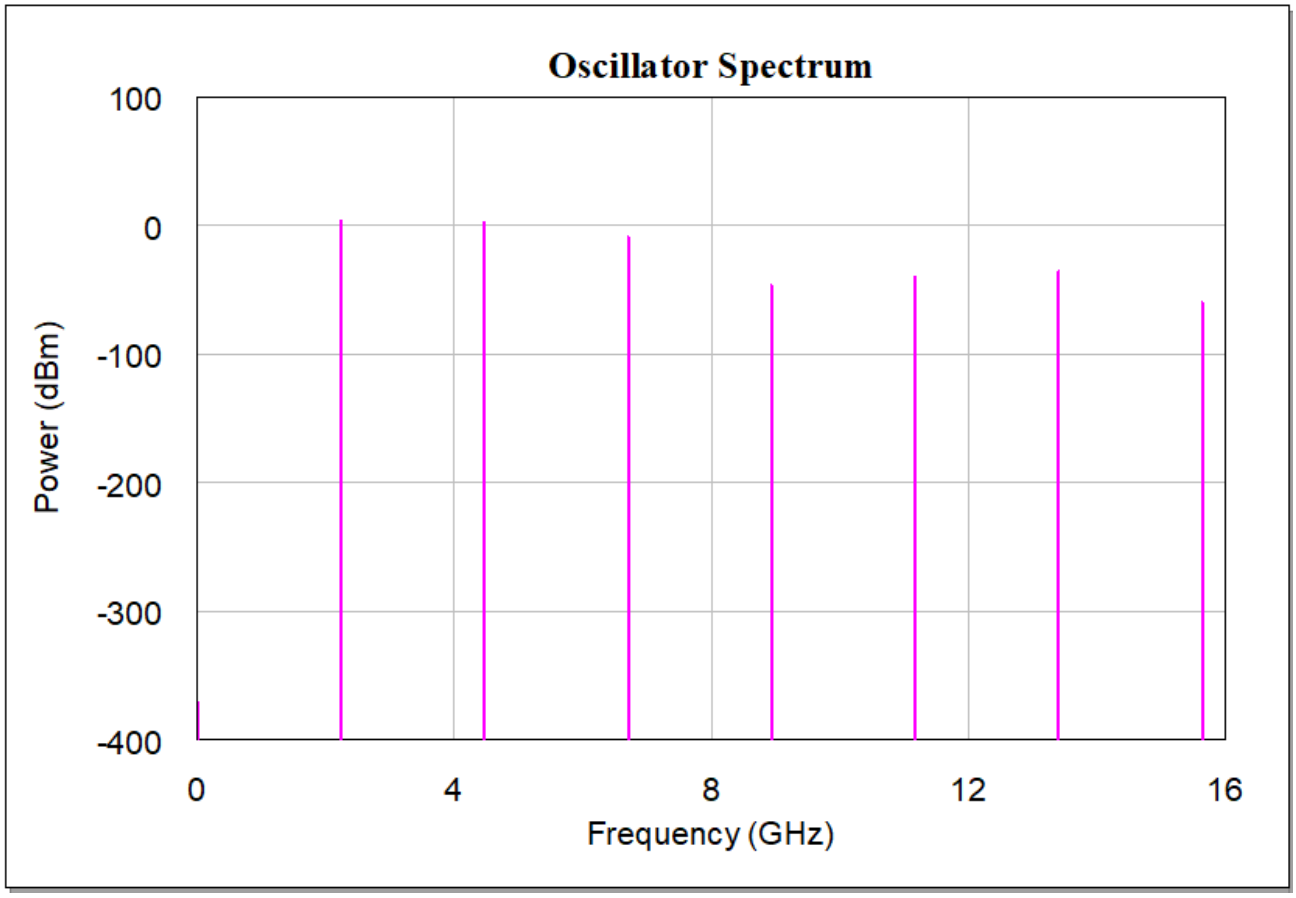


The resulting measurements are now explained:

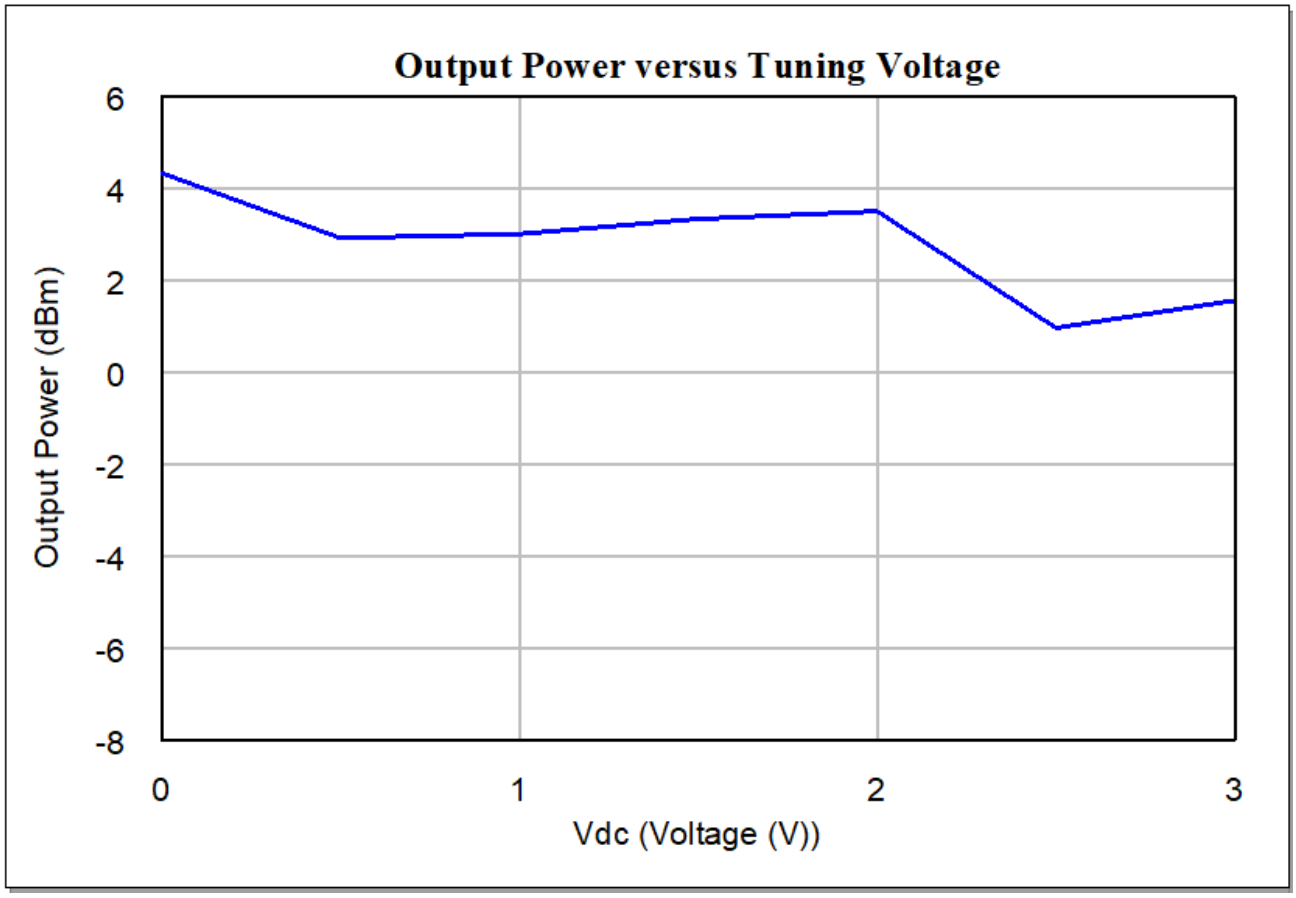
"Oscillation Frequency versus Tuning Voltage" - Plot showing the tuning range of the oscillator by the DC source. The swept voltage setting is used as the x-axis for this graph.



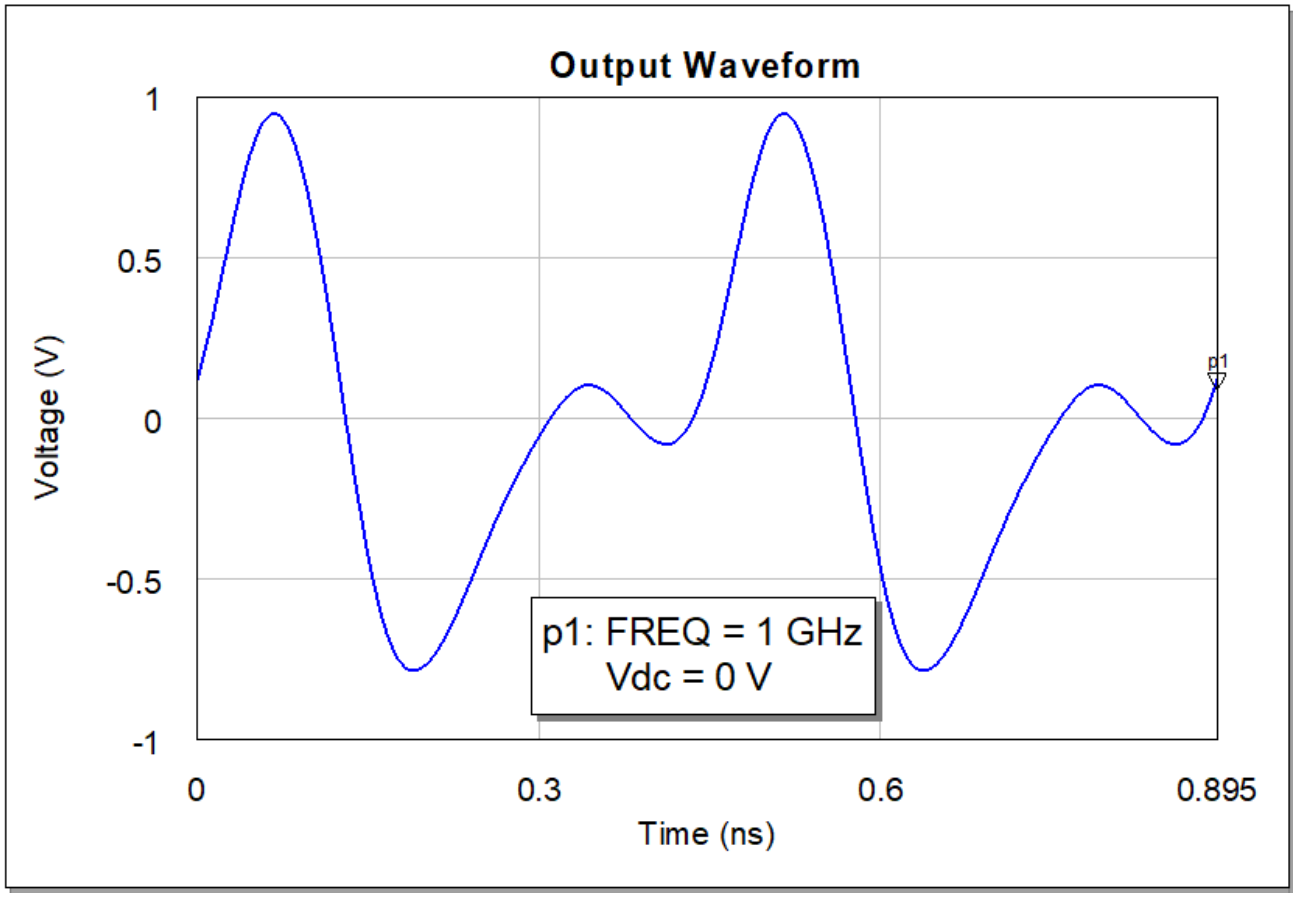
"Oscillator Spectrum" - Plot showing the output power spectrum for the oscillator. This graph is set up to allow the tuner to change the state of the swept voltage source. Tune on the left "Vdc" parameter and watch the spectrum change.



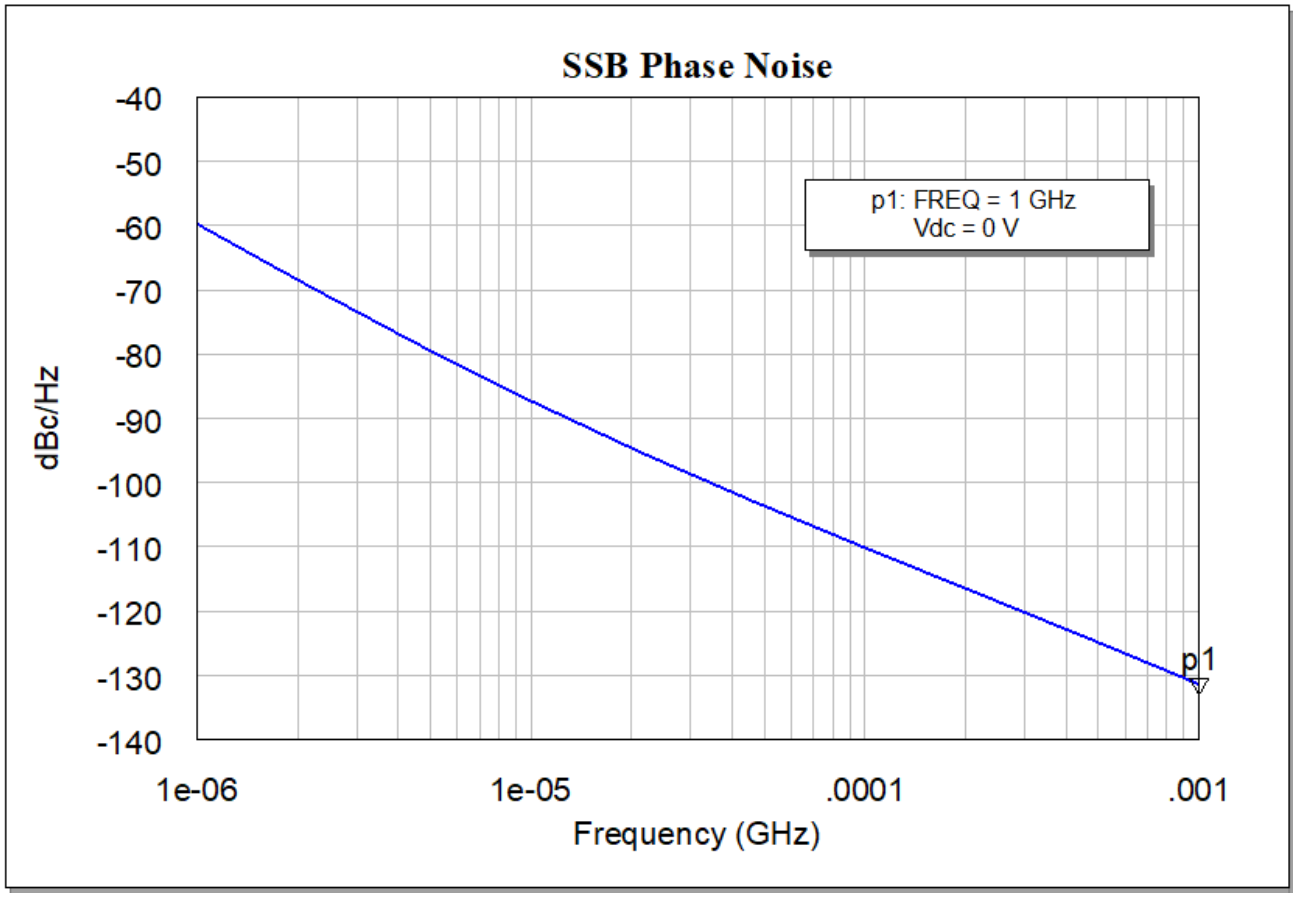
"Output Power versus Tuning Voltage" - Plot showing the output power of the oscillator versus the tuning voltage of the oscillator. The swept voltage setting is used as the x-axis for this graph.



"Output Waveform" - Plot showing the output voltage waveform for the oscillator. This graph is set up to allow the tuner to change the state of the swept voltage source. Tune on the left "Vdc" parameter and watch the waveform change.



"SSB Phase Noise" - Plot showing the single sideband phase noise of the oscillator. This graph is set up to allow the tuner to change the state of the swept voltage source. Tune on the left "Vdc" parameter and watch the phase noise change slightly.



The schematic "3_Varactor_CV_Setup" is used for creating the graph "Varactor Capacitance vs. Tuning Voltage", which shows the capacitance of the varactor as the bias voltage is changed. Note that the measurement models the load as a parallel RC circuit, and plots the (varactor) capacitance.

The schematics "3_Ideal Negative Resistance" and "3_Ideal Tank Circuit" are included for reference. They are the "ideal" schematics before a layout was generated with microstrip elements.