Design Checker

The Design Checker is a collection of checks to look for mistakes in your design that are hard to spot in designs, especially big or complex designs. The utility allows you to configure the checks you would like to run and then displays any errors that were found in either the current project or the active schematic or system diagram.

This utility is configured to run two different ways.

1. The group below will run the script from the AWRDE using the dialog from the utility.
2. There is a form lower down that runs and returns the errors to this page. Any error with a link will browse the program to that error, offering more capability than the previous way to run.

Run Check from the AWRDE

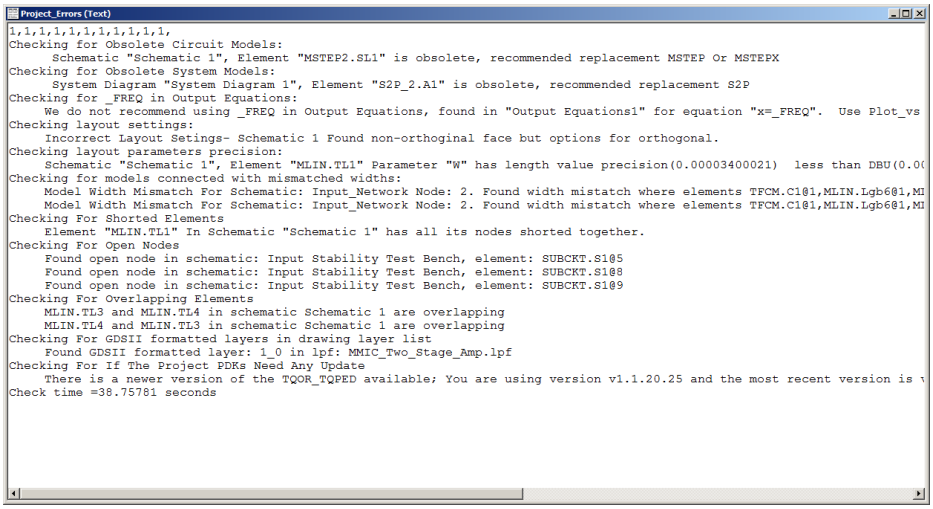
To run this script

Select **Scripts > Project > Design_Checker** from the Menus.

Or, in versions that support the script, you can run the utility directly from this page using this button.

Run Utilit

When the utility is done, a data file named "Project_Errors" is added to your project and opened.



If the data file "Project_Errors" is in the project, the script will remember the last checks you ran and will have those checks enabled in the dialog. Each will overwrite the "Project_Errors" file, you should make a copy of the file if you want to keep results around.

Run Check from this Website

☑Obsolete Circuit Models (recommended replacement listed)
☑Obsolete System Models (recommended replacement listed)
☑ _FREQ in Output Equations (recommended equation solution listed)
☑Layout Options (list options needed for layout style found)
☑Model Layout Precision (list layout parameter with more precision that the DBU)
☑Mismatched Widths (check for connected models with widths that are not matched)
☑Shorted Circuit Elements (list models with all nodes shorted)
☑Open Circuit Nodes (list models with nodes not connected)
☑Overlapping Circuit Elements (list models that are completely overlapping)
☑GDS Formatted Drawing Layers (Lists any GDSII formatted Drawing Layers)
☑PDK Version Check (Checks the existing PDKs and see if there is a newer version available)
How Much to Check
Entire Design
Active Schematic/System Diagram

Run Desi

Review Results

Error Types Descriptions

Obsolete Circuit Models

This check will look for any circuit model that is now considered obsolete and recommend an different model to use. Typically these models issue a warning when simulated but the warning is easy to miss. As a designer you should decide if the obsolete model is okay to continue using in your design.

Obsolete System Models

This check will look for any system model that is now considered obsolete and recommend an different model to use. Typically these models issue a warning when simulated but the warning is easy to miss. As a designer you should decide if the obsolete model is okay to continue using in your design.

_FREQ in Output Equations

Many times while writing output equations, you will want to also get the frequencies associated with any measurement (or any other measurement's x-axis values). People have used _FREQ built in variable in the past. This variable can change based on simulation order which means equations that work at one point could not work when a design changes. The better approach is to the "swpval(x)" function where x would be the result of an output equation.

Orthogonal Layout Mode

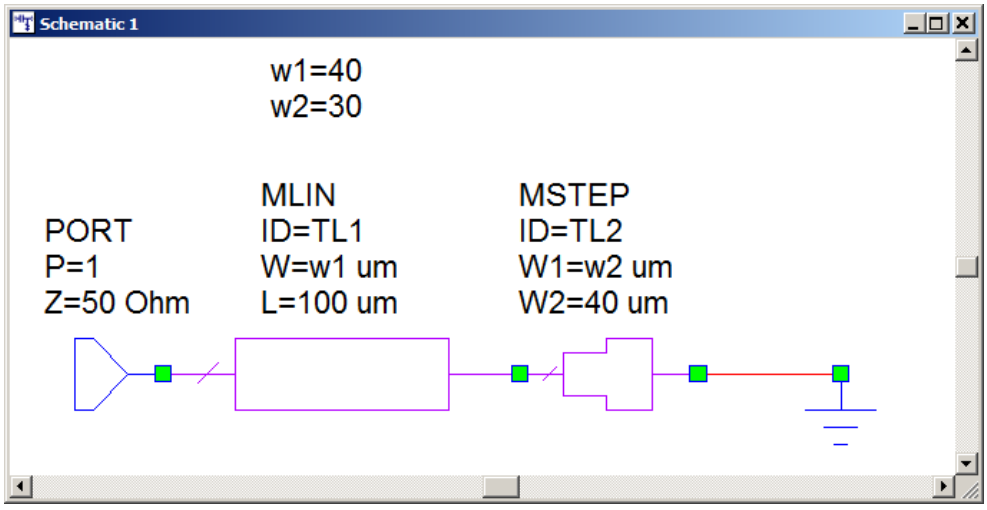
There are several layout options available on the **Options > Layout Options** and the Layout tab that help designs not have gaps in layout when building hierarchical designs. The right settings depend on if your layout is orthogonal or not. We find that many designers are not sure which mode they are in and so this check will determine if your layout is orthogonal or not and which options to change if needed.

Model Layout Precision

Many times model parameters can have more precision that the data base unit size of the layout. This typically is not a problem but might cause layouts to not properly snap together.

Mismatched Widths

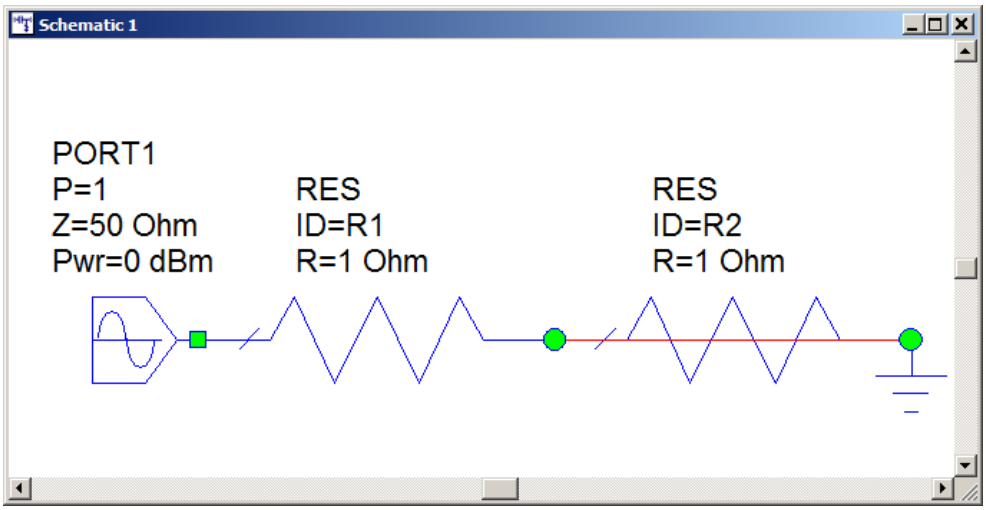
This checks for any models that are connected that have widths parameters that do not match. We prefer users to use intelligent models (where a model can get its width from the model it is connected to), however many customers do not and can have data entry errors where widths of connecting models should match but do not. For example, when using equations, it is possible to type the wrong equation values as shown below.



This check will report any elements that were found in this condition.

Shorted Circuit Elements

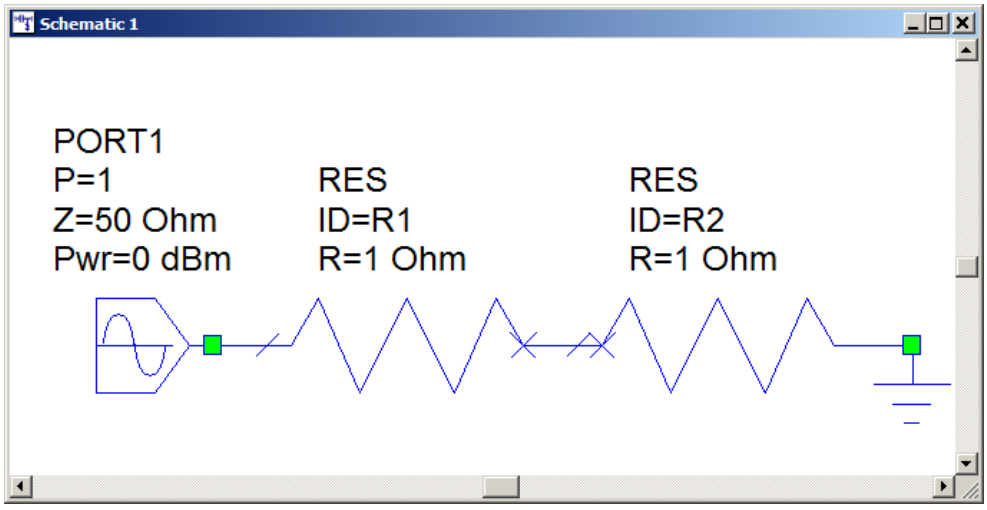
This checks for any models that are enabled but have all of their nodes shorted together. This condition is typically a case where a designer intended to disable an element and did not.



This check will report any elements that were found in this condition.

Open Circuit Elements

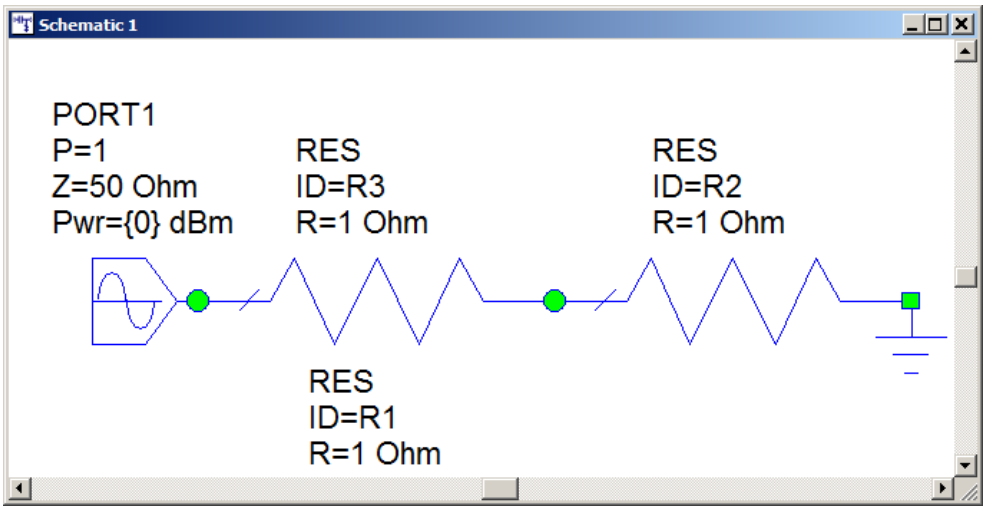
This checks for any models that are enabled and have nodes that are not connected to anything. This condition is typically a case where a designer overlapped nodes to connect them and miss placed a part. The picture below shows this case where the nodes of both resistors are not overlapped. In a big schematic this error would be difficult to spot.



This check will report any elements that were found in this condition.

Overlapping Circuit Elements

This checks for any models that are exactly on top of one another. The picture below shows this case where the left resistor looks like there is one resistor, but actually there are two that are exactly overlapping.



This check will report any elements that were found in this condition.

GDS Formatted Drawing Layers

This checks for any drawing layers using GDSII formatted drawing layer names. This typically happens when using a model or importing an artwork cell where the correct layers are not already setup. The drawing system will automatically add the layers as drawing layers and model layers. Typically designers like to keep the drawing layer list clean for the named layers they understand for their process. The typical fix is to go into the model layer mapping and map the same model layer to a different drawing layer for your process and then delete this drawing layer.

PDK Version Check

This checks for if there are any newer PDKs available for the existing PDK's in the project. The check goes through each existing PDKs one by one and then goes through the AWR PDK Availibility library in the vendor libraries and see if there is a newer version of the PDK available. Then it informs the user of the result. You need to have internet connection to run this check.