MMIC_Bias_Voltage_Regulator

Where To Find This Example

Select **Help > Open Examples...** from the menus and type either the example name listed above or one of the keywords below.

Or in Version 13 or higher you can open the project directly from this page using this button. Make sure to select the **Enable Guided Help** before clicking this button.

Open Install Example

Design Notes

MMIC Gate-Bias Voltage-Regulator Example

In this project, three MMIC gate-bias voltage-regulators were designed, simulated and compared in terms of variation compensation. RF FET current density, regulated voltage, gain and regulator power dissipation are compared in different cases.

Overview

Due to temperature and fabrication process variations, different parameters in the FET, such as pinch off (threshold) voltage and drive current, deviate from their desired design values. The three sample regulator designs in this project compensate for these effects to some extent while simplifying the function assembly and use. Maximum tolerable power dissipation, available supply voltage rails and layout size limitations are some of the constraints which affect final regulator performance. In this project, the regulator power dissipation is limited to 25mW and the bias rail is assumed to be -5V. The three sample circuits in this project show almost similar behavior. The overall layout sizes are also alike. *It is important to emphasize that, the variation compensation performance can be significantly improved mainly at the cost of higher power dissipation.*

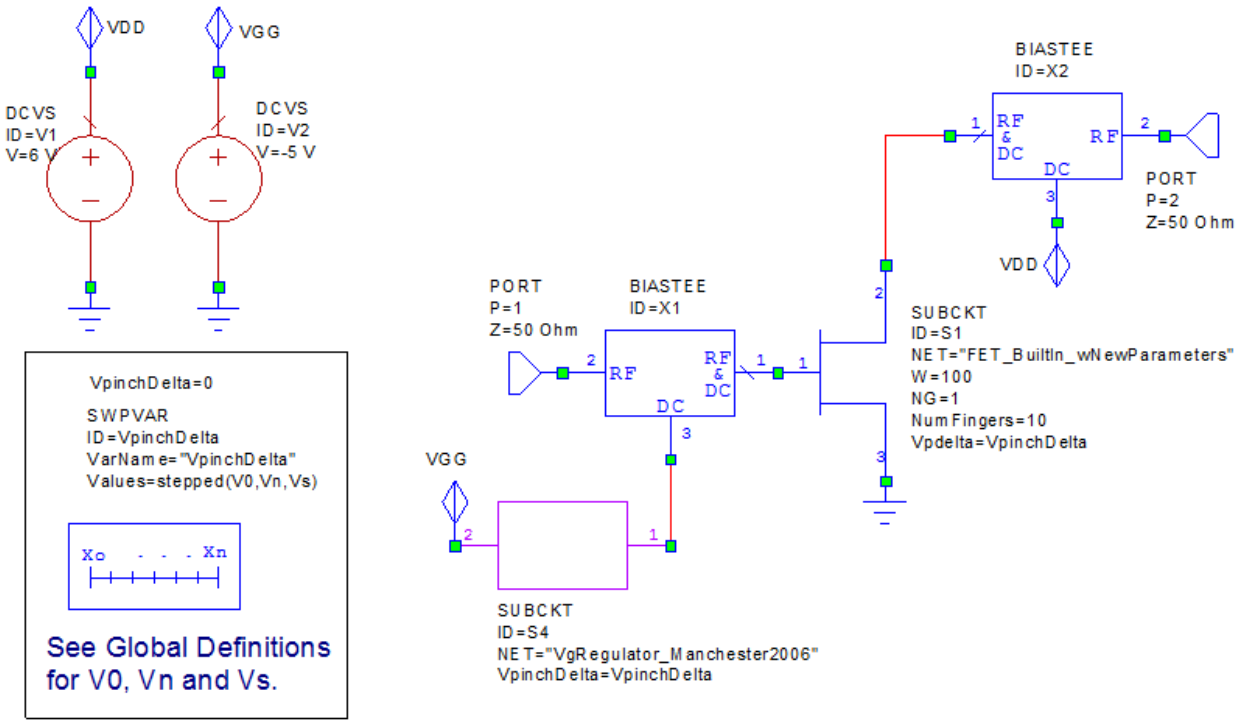
Curve Slope Equations

The slopes of the drain-source current density and regulated gate voltage with respect to pinch off voltage variation as well as drive current variations are calculated as output equations.

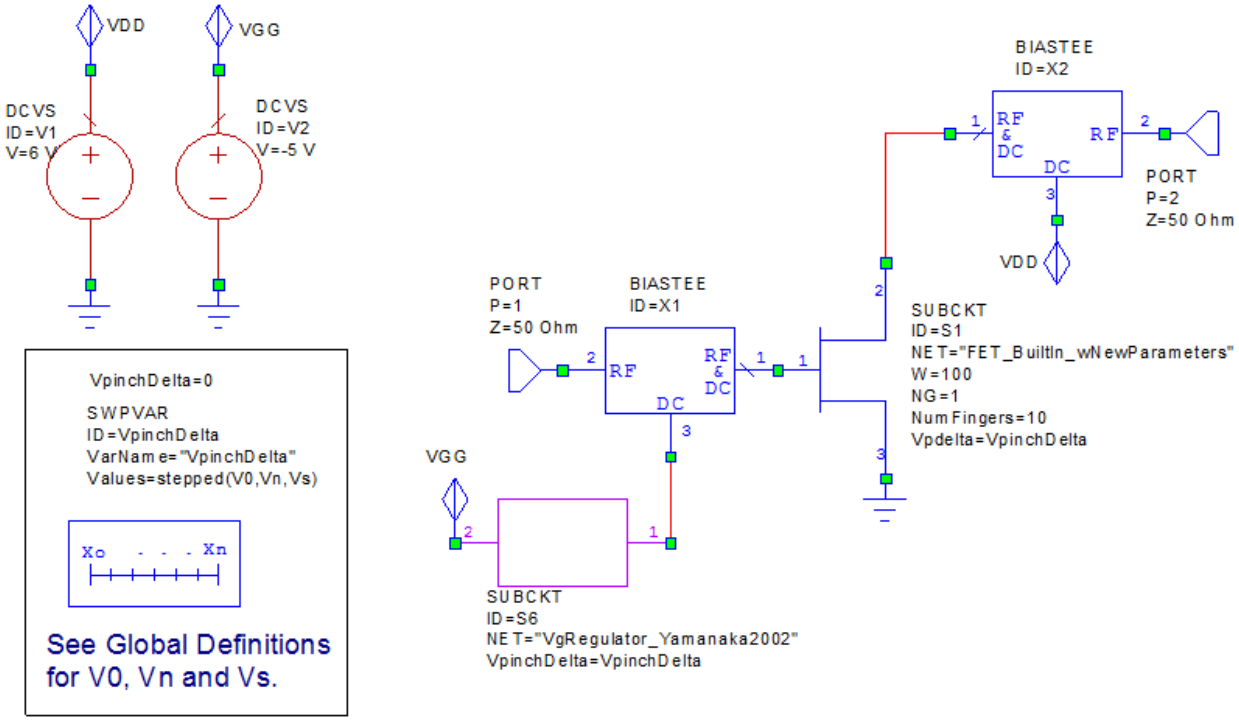
Optimization

There are several parameters and variables in each circuit; thus, one can find a group of designs with similar performance for each of the three configurations. Setting optimization goals limits the number of solutions to those which are more desirable. This project focuses on variation curve slope (as flat as possible), power dissipation (<25mW) and regulated gate voltage(-0.25V) as optimization goals.

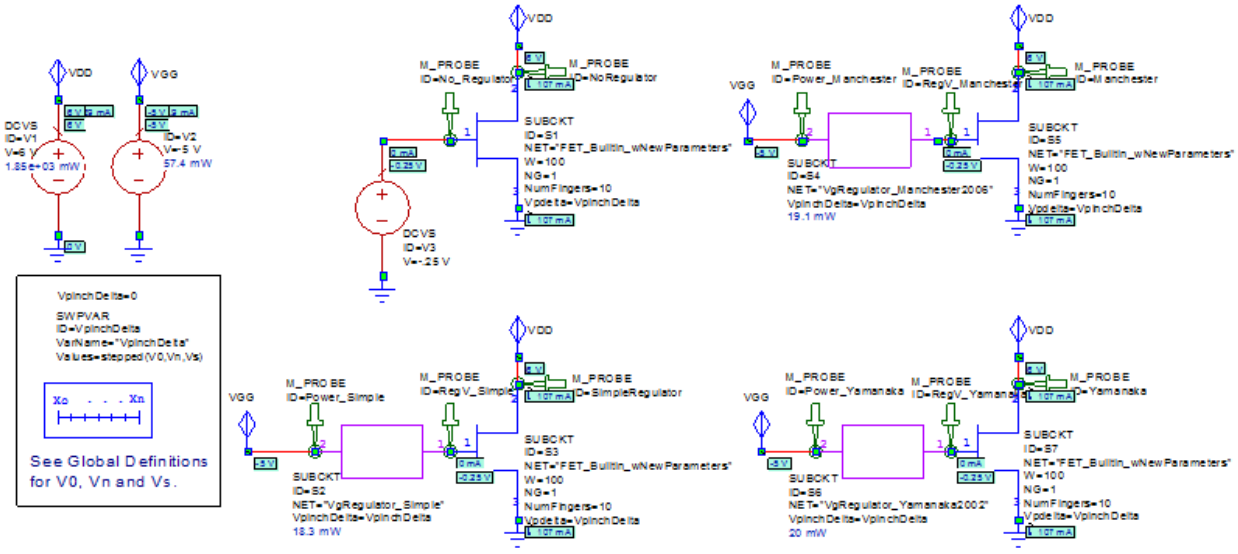
Schematic - TestBench_Vpvaration_Gain_Manchester2006



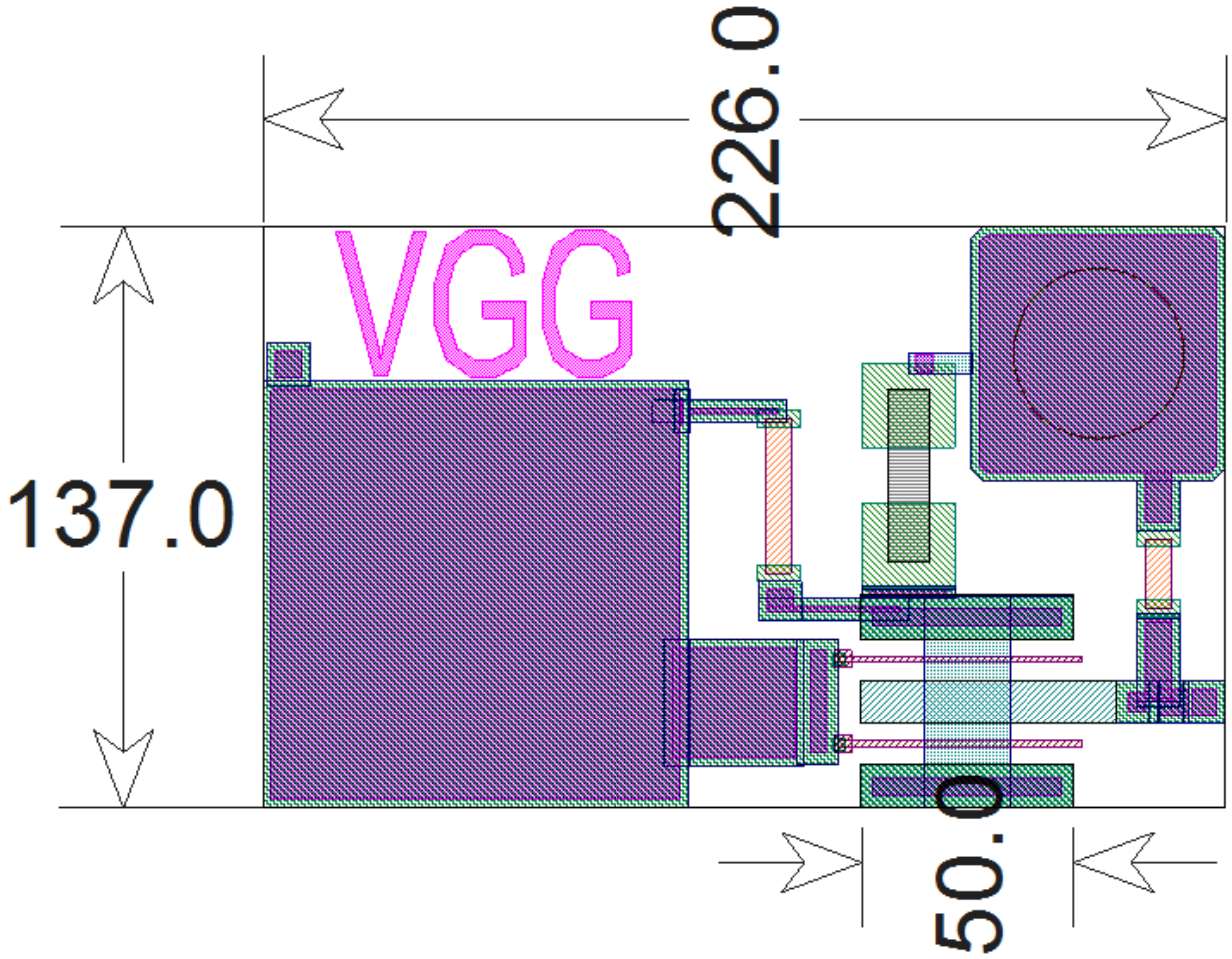
Schematic - TestBench_Vpvaration_Gain_Yamanaka2002



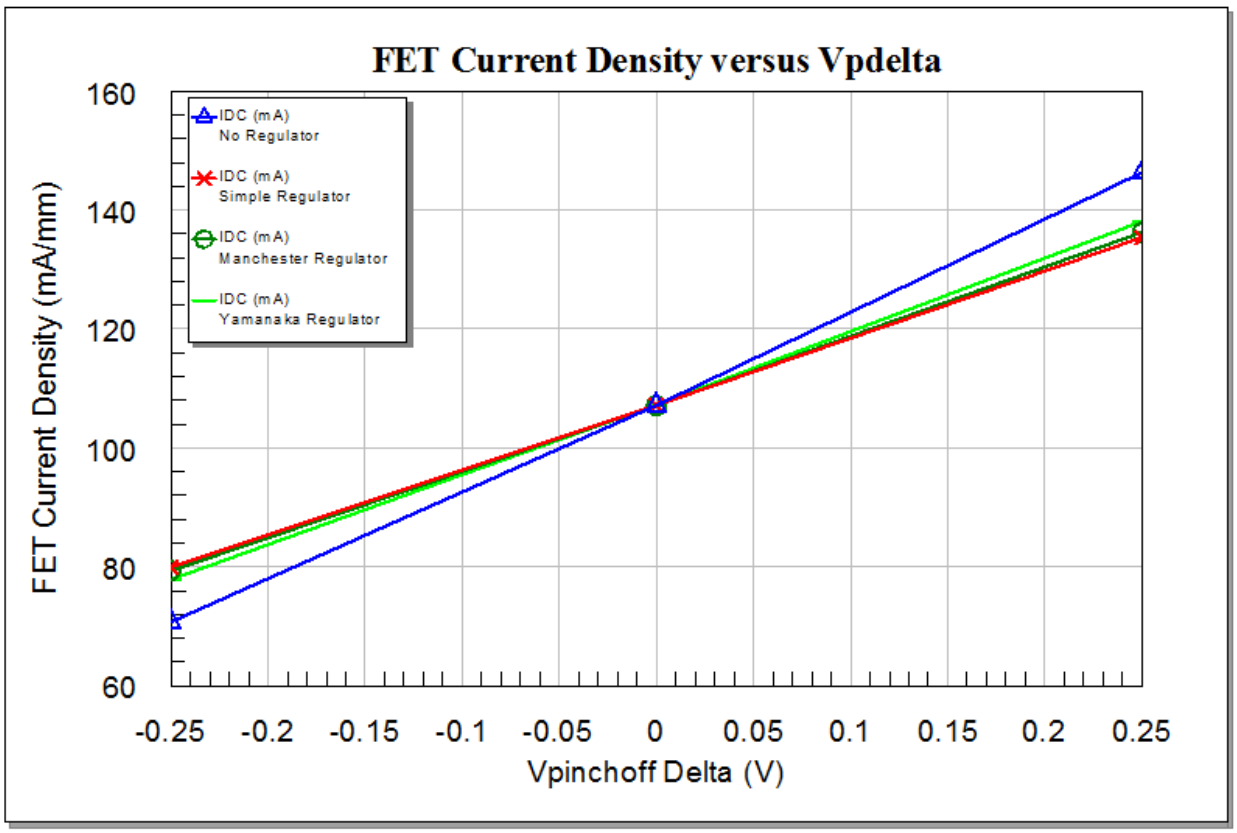
Schematic - TestBench_Vpvaration



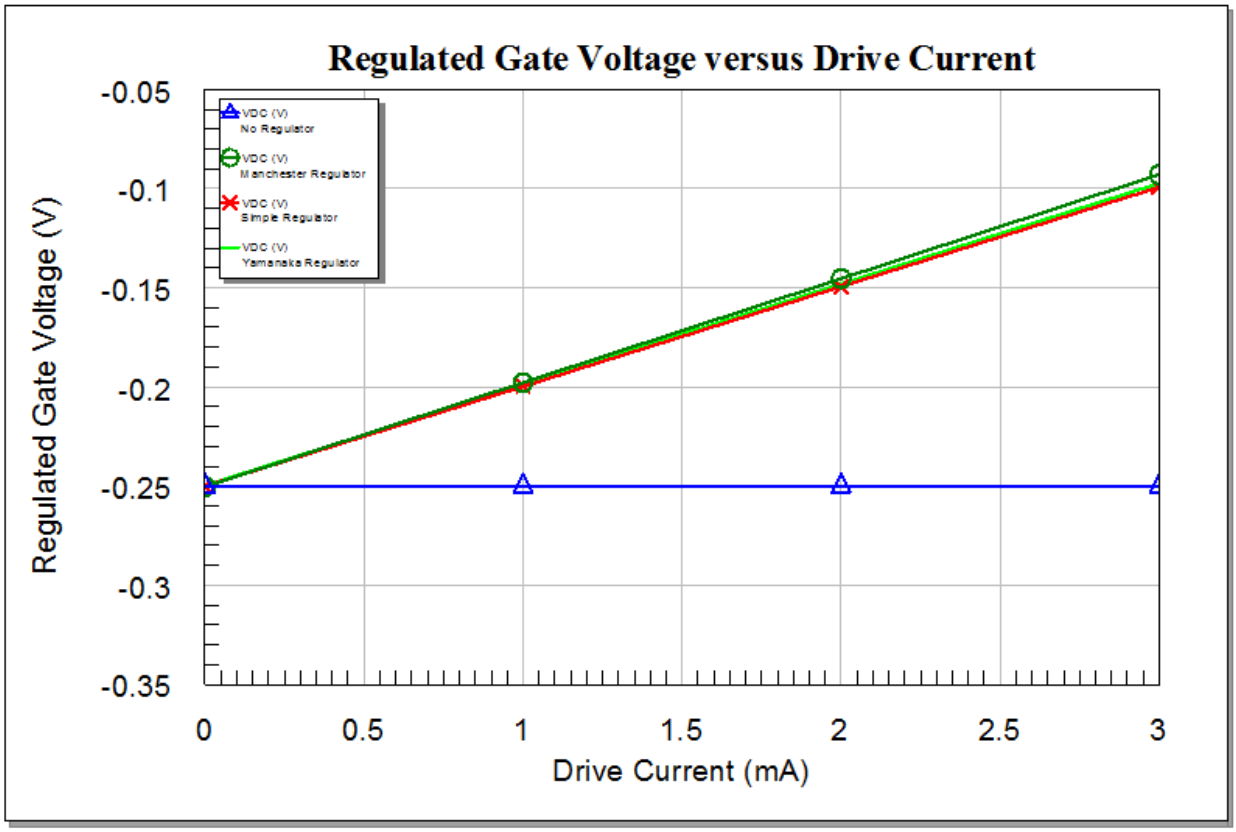
Schematic Layout - VgRegulator_Manchester2006



Graph - FET Current Density versus Vpdelta



Graph - Regulated Gate Voltage versus Drive Current


Regulated Gate Voltage versus Drive Current
Regulated Gate Voltage (V)
-0.05
-0.1
-0.15
-0.2
-0.25
-0.3
-0.35
0
0.5
1
1.5
2
2.5
3
Drive Current (mA)
VDC (V)
No Regulator
VDC (V)
Manchester Regulator
VDC (V)
Simple Regulator
VDC (V)
Yamanaka Regulator