MMIC_Two_Stage_Amp

Where To Find This Example

Select **Help > Open Examples...** from the menus and type either the example name listed above or one of the keywords at the bottom of this page.

You can also open the project directly from this page using this button. Make sure to select the **Help > Enable Guided Help** from the menus before clicking this button.

Open Install Example

Design Notes

MMIC TWO STAGE AMPLIFIER

This is a two stage MMIC amplifier example that demonstrates many of the benefits using Microwave Office for GaAs MMIC design:

Em Extraction using AXIEM and Geometry Simplfication

Multi-Layer Metalization - Line Types

Intelligent Interconnects

MTRACE2 - Routeable MLIN

Electrical editing in Layout

Layout checking for connectivity and DRC

Face Offsets

Snap to Fit

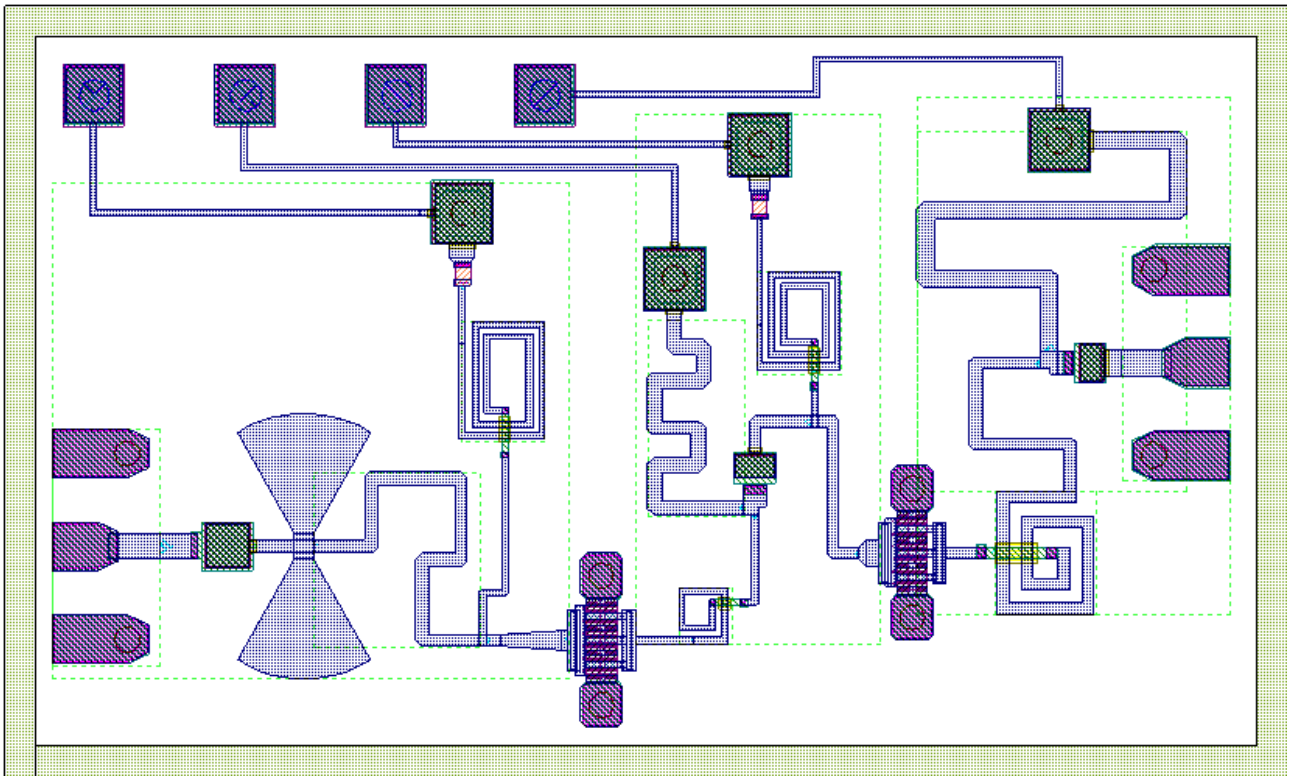
DRC

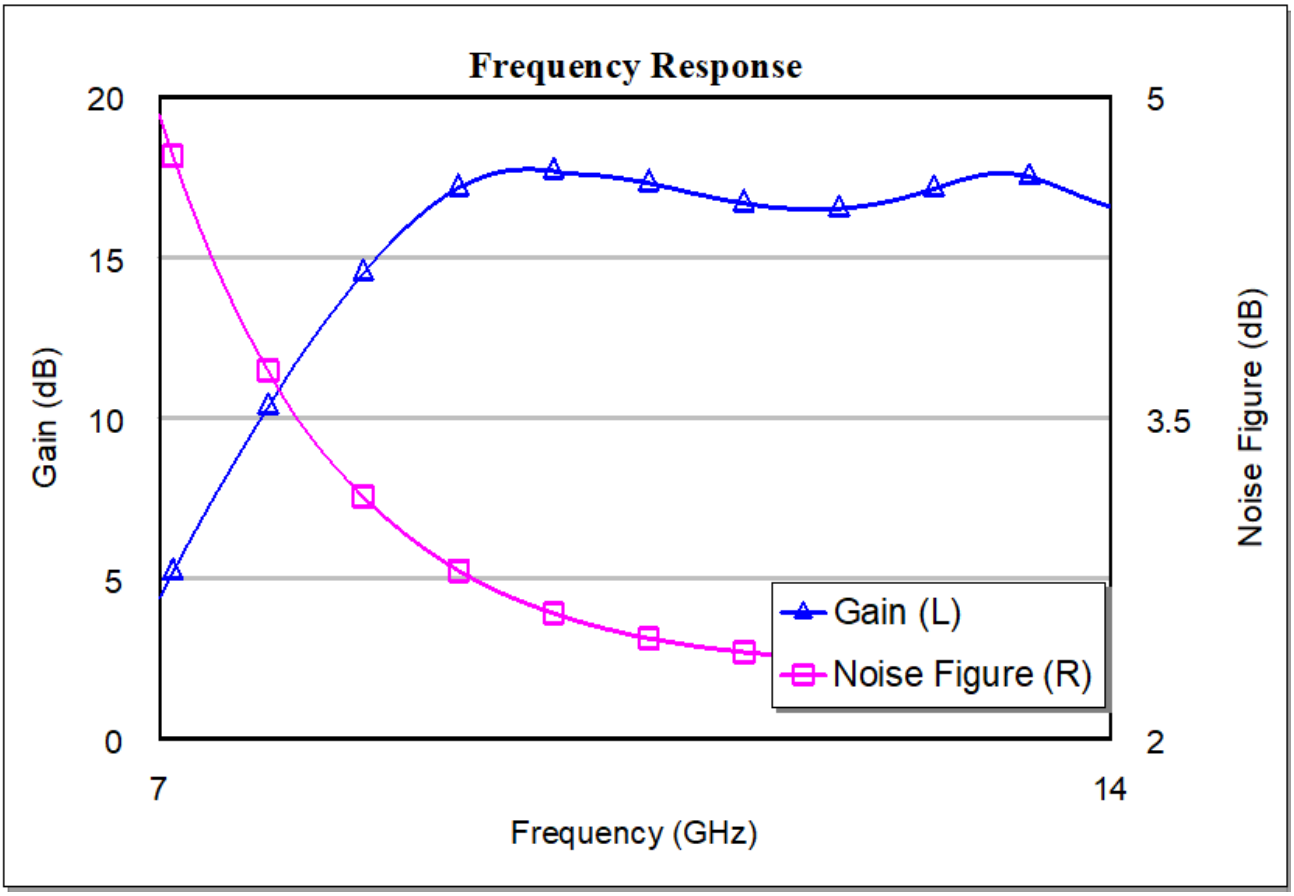
Switch Views

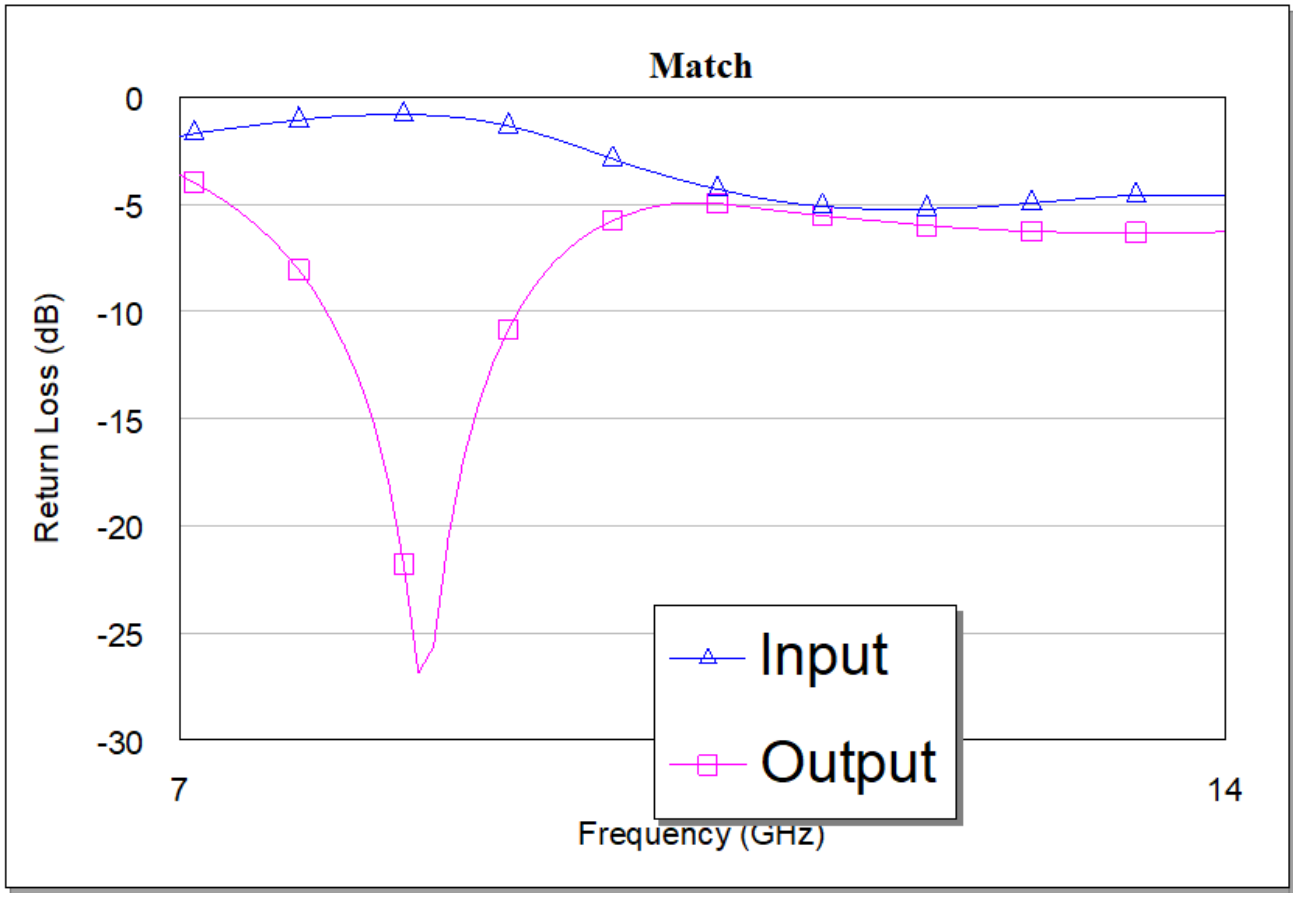
Gamma Probes for internal stability analysis

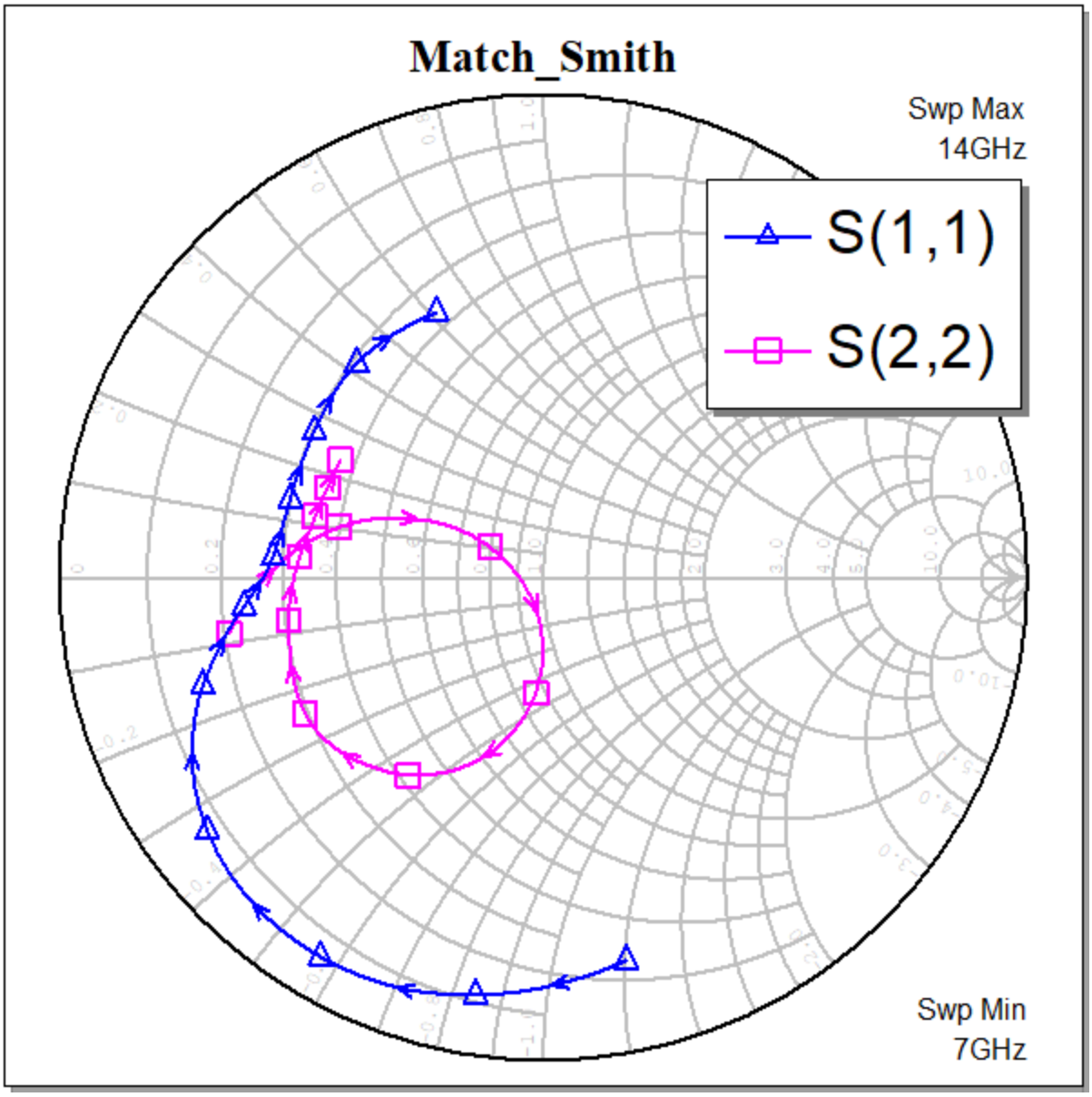
Overview

This project shows the design of a 10-12 GHz MMIC Amplifier built using a generic AWR MMIC process. The amplifier has nominal gain of 17 dB. The design is set up for tuning the input and interstage matching networks. Bring up the tuner (**Simulate > Tune**) and drag the sliders up and down to view the impact of parameter changes on the "Frequency Response" and "Match" Graph




Frequency Response
20
15
10
5
0
5
3.5
2
7
14
Gain (dB)
Noise Figure (dB)
Frequency (GHz)
Gain (L)
Noise Figure (R)


Match
0
-5
-10
-15
-20
-25
-30
Return Loss (dB)
7
14
Frequency (GHz)
Input
Output



Label Project Name, Date, and Time

For any schematic or graph if you add text (**Draw > Add Text**) with the exact names, Project:, Time:, or Date: (notice the semicolons). You can run a script to fill in that information. Select **Scripts > Global Scripts > Project > Label_Time_Date_Project_Name**.

In this project, these text strings are on the **Two_Stage_SS_Amp** schematic in the lower right corner, run this script to see these values appear. You may have to zoom to see the text after the script runs.

Switch Views

Switch Views and Switch Lists provide an easy way for a designer to toggle between different versions of a model while maintaining a single layout cell for that instance. In this project, Switch Views are used to create alternate LVS versions of subcircuits.

For this project, the most important benefit of Switch Views and Switch Lists is how much they simplify having multiple models for the same circuit part(s). This example uses Switch Views to create alternate views of elements for LVS (Layout versus Schematic) netlisting.

Switch Views In This Project

Microstrip inductors in the in the design have alternate LVS switch views.

EM Extraction with AXIEM

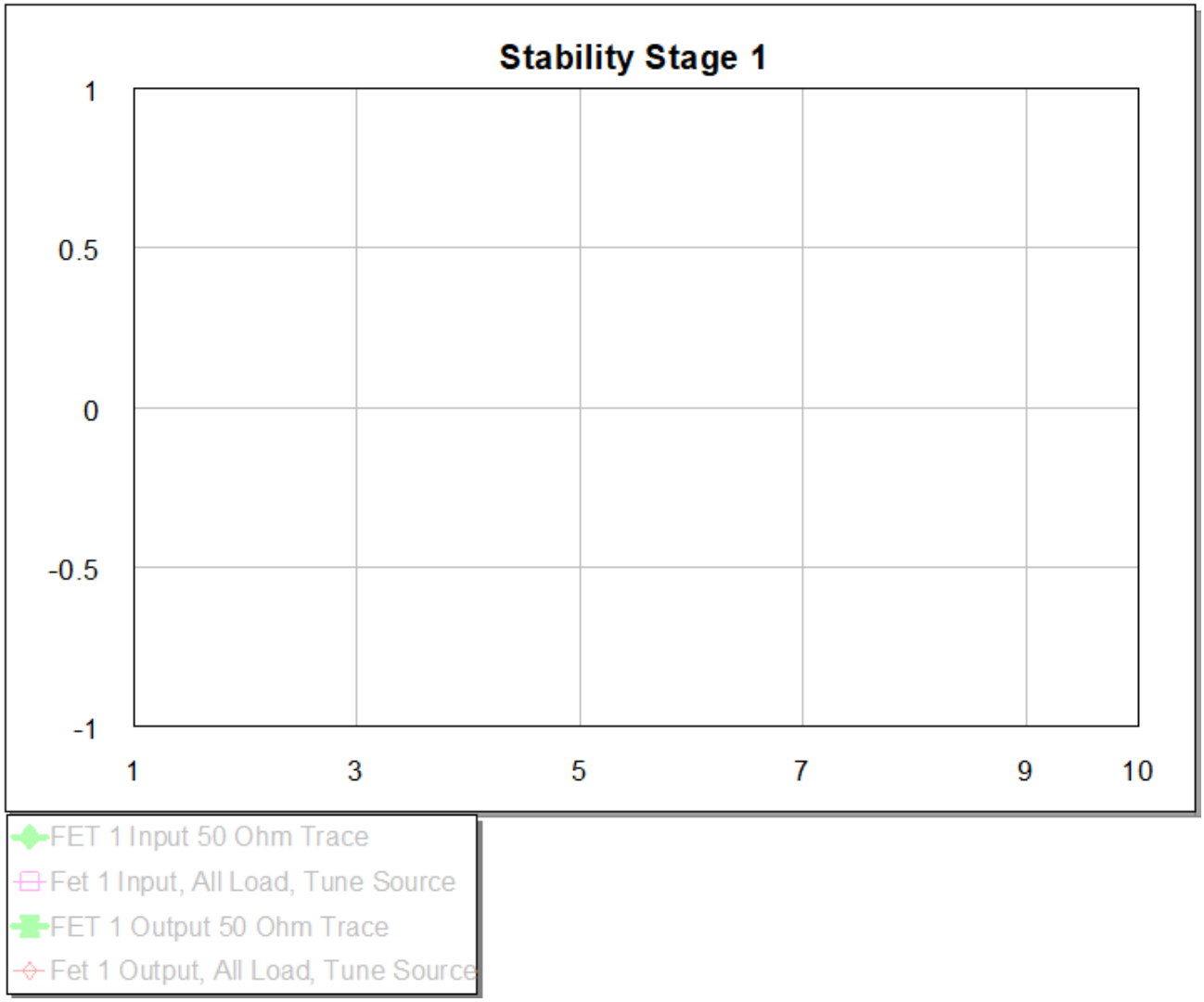
You can also use EM Extraction to toggle between circuit models, and EM simulation results.

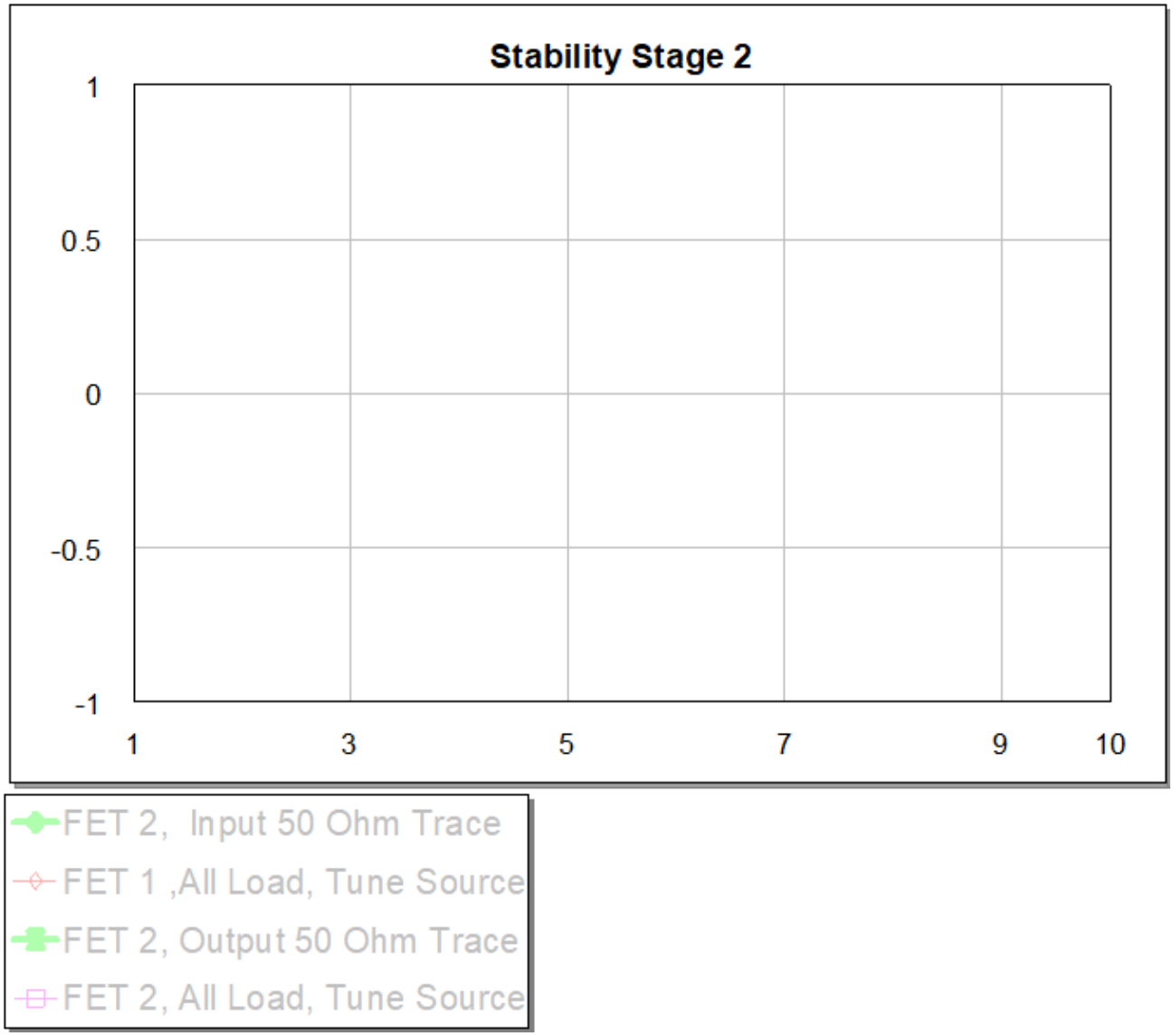
This project has been also configured to use EM Extraction to simulate the entire design using AXIEM. Please see the **Help** for extraction setup details as this example will focus on the results rather than the setup details. To see AXIEM simulate the metal, enable the EXTRACT block on the "Linear_Test_Bench" schematic. Alternatively, you can enable the EXTRACT blocks in the individual matching network schematics to see the effects of EM simulation of just those sections.

Geometry Simplification rules are used in this project to transform layout from shapes needed for manufacturing (what is taped out) to shapes that are most efficient for EM simulation. To see this, enable one of the extract blocks, right click on the extract block and select **Add Extraction**. This will generate an EM document in the project, then right click on the EM document and select **Preview Geometry** to see the simplified shapes in the layout. Pay close attention to how the air bridge shapes for inductors or capacitors are done and what the bond pads and vias look like. These rules are setup in the STACKUP element in the Global Definitions window.

Gamma Probe Stability Analysis

Graphs named "Stability Stage 1" and "Stability Stage 2" plot the stability index of the amplifier with swepted input and output impedances. All of the load impedances are plotted, and the tuner is used to change the source impedance. After simulation, use the tuner to vary the source impedance angles and look for any value > 1 for potential instability. The core design in the "Two_Stage_SS_Amp" schematic has gamma probes at the input and output of each transistor to perform this analysis.


Stability Stage 1
1
0.5
0
-0.5
-1
1
3
5
7
9
10
FET 1 Input 50 Ohm Trace
Fet 1 Input, All Load, Tune Source
FET 1 Output 50 Ohm Trace
Fet 1 Output, All Load, Tune Source



Multi-Layer Metalization

Microwave Office uses the concept of **Line Types** to automatically draw multi-layer metal lines. Open the layout view of the "Input Network" schematic. Select the **MTRACE2** between the input capacitor and the radial stubs. Right click and select **Shape Properties** to open the **Cell Options** dialog box. Click on the **Line Type** drop down box and change the Line Type to **"Plated Metal Line"**. Notice how the line automatically draws in all of the layers with the correct offsets. Additional Line Types can be added to the project by editing the **Layer Process File** (.lpf) in a text editor. See the online User Guide for a full description of the Layer Process File (**Help>Contents and Index**).

Intelligent Interconnects

From the "Input Network" layout, select the line between the input capacitor and the radial stubs. Change the **MTRACE2** Line Type to **"Cap Bottom Line"** and notice how the connection to the top of the capacitor automatically adds a via to connect the plated metal to the cap bottom layer. The intelligent interconnect draws the proper interconnect according to the DRC rules so the user does not have to remember all of the subtle rules. From the "Input_Network" schematic, delete the wire connecting the input capacitor to the **MTRACE2** element. Notice how the connection to the top plate disappears when the capacitor is not connected to anything. The Intelligent Interconnects are provided with the Foundry Libraries supplied by AWR.

Electrical Editing in Layout

Open the layout view of the "Input_Network" schematic and double-click on the input capacitor. Eight drag handles will appear in the layout to adjust the size of the capacitor. Pull one of the drag handles in the corner to make the capacitor larger. Notice that the width and length in the schematic have been updated and the value of the capacitance has changed to reflect the new size of the capacitor. Move one of the drag handles on the side of the capacitor and notice that the capacitance stays constant. The drag handle editing and update of the electrical schematic is a unique feature of Microwave Office that allows the user to make changes in the layout without worrying about keeping the layout and electrical schematic synchronized.

Face Offsets

From the "Two Stage SS" layout, select the **DC Bondpad** furthest to the right side. Right click, select **Shape Properties**. From the **Cell Options** dialog box, press the **Faces** tab to bring up the Face options for the **DC Bondpad**. Select **"Face 2"** from the Face drop down box. Notice how the selected face appears in blue on the layout. Select **"Offset"** under the **Face Justification** area and enter **"-25"** in the **Offset dx** box. The center of Face 2 has now moved 25um higher in the layout. Now that the face center has changed, a **red X** appears in the layout to let the user know that the layout is not connected properly. You can also set the face to be variable and the line can connect anywhere along the bond pad. See the online User's Guide for more information on Face properties.

Snap to Fit

Select the **MTRACE** connected to face 2 of the **Bondpad**. Press the **Snap to Fit** button at the top of Microwave Office. Notice how the **MTRACE2** element automatically adjusts itself to make the proper connection. The **MTRACE2** and **MCTRACE** elements have this special property to adjust their size to complete a connection. This is very useful when routing bias lines to **DC Bondpads**.

Schematic Connectivity

The AWR Design Environment contains a connectivity checker capability. This is similar to LVS. Open the "Linear_Test_Bench" schematic and press the **New Schematic Layout View** hot button along the top of Microwave Office. Select **Verify > Run Connectivity Check** from the toolbar to run the check. A dialog will open to display any errors. The project is shipped connectivity clean. Open any layout window and draw shapes to short out shapes or move layout objects to make open circuits and run the check again to see how errors are reported.

DRC

Open the "Input_Network" schematic and press the **New Schematic Layout View** hot button along the top of Microwave Office. Select **Verify > Design Rule Check** from the toolbar to open the DRC rules dialog window. From the DRC rules dialog window, press the **Run DRC** button to start the DRC rules check on the layout of the "Input Network". A DRC rules violation window displays the DRC violation. Double-click on the DRC violation and the error will be highlighted in red in the layout window. Press the **Clear Errors** button to stop the DRC engine. See the online User's Guide for all of the DRC rules. Use a text editor to open the **"drc_rules.txt"** file located in the Microwave Office directory. After editing the **"drc_rules.txt"** file, press the "Load Rules File" button to load the updated rules and run the DRC again.